



Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1450-06

PCB:



PCB 2VR LA-J521P REV1 M/B NVIDIA N18E
DAB006V010
PCB@

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Schematic Document

(Viper Comet Lake H with nVIDIA N18E)

P1151

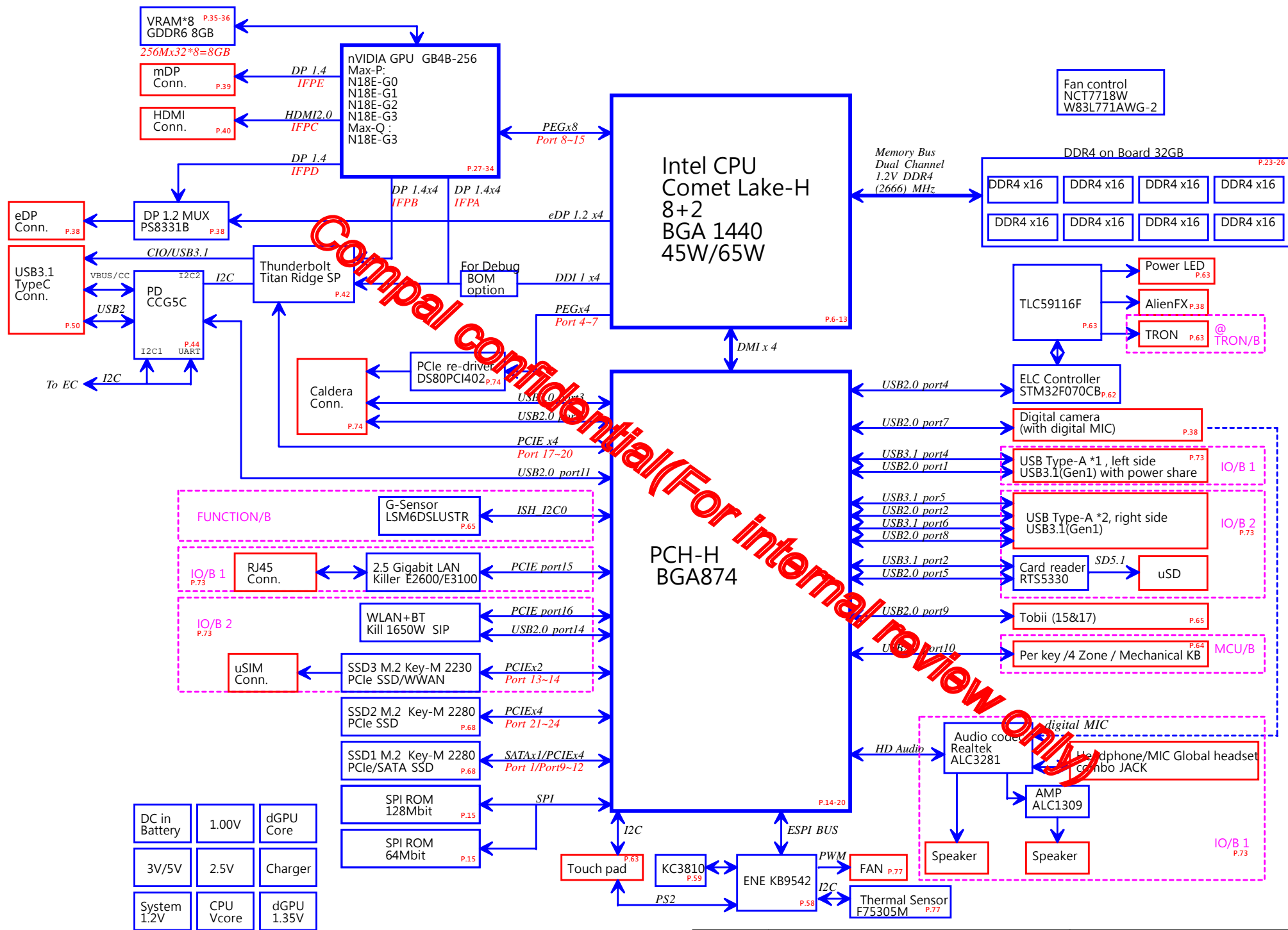
2020-04-09

Rev: 1.0 (A00)

BOM Structure

PCB@ : PCB PN
PCH@: PCH P/N
EC@: EC Chip P/N
NV@: BIOS board ID (GPU type)
N18EG0@/N18EG1@/N18EG2@/N18EG3@/N18EG1B@: GPU_ID & GPU Chip
TYPEC@/RTD3@: TBT
G0G1G3Q@/G1G2@/G3P@: OVR(NV)
NG3P@: OVRM(ARD request)
LCDTESTEC@: LCD Test
CMC@: CMC Debug Port
128@: 16M ROM Sch
RF@/EMI@/ESD@/ TYPEC@RF@ : EMI, ESD and RF Component
CML@: CML platform
CONN@:Connector
DDP16G@/SDP8G@: DDR4 DDP & SDP
SAM8G@/HYX8G@/MCN8G@/MCN8G1@/SAM16G@/HYX16G@/MCN16G@/MCN16G1@/SAM32G@/MCN32G@:
DDR4 Chip
S_8G@/H_8G@/M_8G@/M_8G1@/S_16G@/H_16G@/M_16G@/M_16G1@/S_32G@/H_32G@/M_32G@: PCH DDR4 ID
Strap pin
@RTD3@/@TBT@:TBT RTD3 Un-POP Component
HMO16S32@: Hynix/Micron old die 16G & S32G T7 pin
MCNGD8A@/MCNGD6A@/SAMGD6A@/SAMGD8A@:VRAM CHIP
VRAM_S@/VRAM_M@: VRAM strap pin
@: Un-pop Component

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Board ID Table for AD channel

Vcc 3.3V +/- 1%					
Ra 100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.201V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.546V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	1.2M +/- 1%	3.020V	3.046V	3.067V	0xFF

PCIE CLK table

PCIE CLK	PCB Revision
0	GPU
1	SSD2
2	SSD3/WWAN
3	TBT
4	LAN
5	WLAN
6	caldera
7	SSD1

Board ID table

NV			AMD	PCB Revision
N18P	N18E			
	2Stage	1Stage		
0	4	8	12	EVT-1
1	5	9	13	DVT-1
2	6	10	14	DVT-2
3	7	11	15	Pilot

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

PCH-H CM246

HSIO	USB3.1	PCIe	SATA3	Function	
0	1				
1	2			Card reader	
2	3			Caldera	
3	4			JUSB3 left side	
4	5			JIO right side USB2	
5	6			JIO right side USB1	
6	7	1			
7	8	2			
8	9	3			
9	10	4			
10		5			
11		6			
12		7			
13		8			
14		9		JSSD1, 2280 SATA/PCIe x4	
15		10			
16		11	0a		
17		12	1a	WWAN JSSD3 PCIe X2	
18		13	0b		
19		14	1b	LAN	
20		15	2	WLAN	
21		16	3	TBT PCIe X4	
22		17	4	JSSD2, 2280 PCIe x4	
23		18	5		
24		19			
25		20			
26		21			
27		22			
28		23			
29		24			

USB2	Function
1	JUSB3 left side
2	JIO right side USB1
3	Caldera
4	ELC
5	Card reader
6	WWAN
7	Camera
8	JIO right side USB2
9	Tobii
10	Per Key
11	Thunderbolt PD
12	Tron light
13	
14	Bluetooth

Symbol Note :

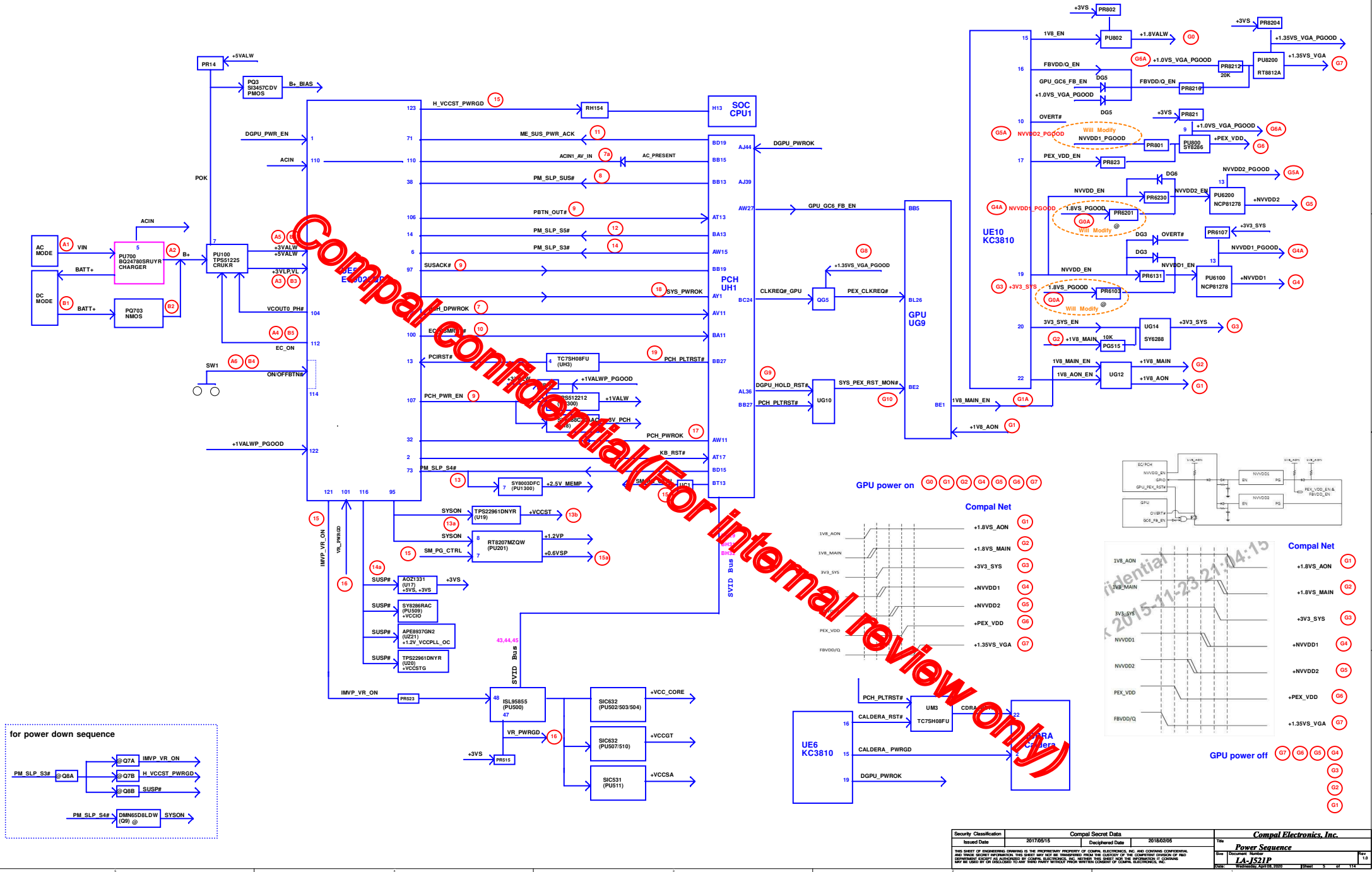


Digital Ground



Analog Ground

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Caldera TX

GPU TX

Caldera RX

GPU RX



CPU R1:

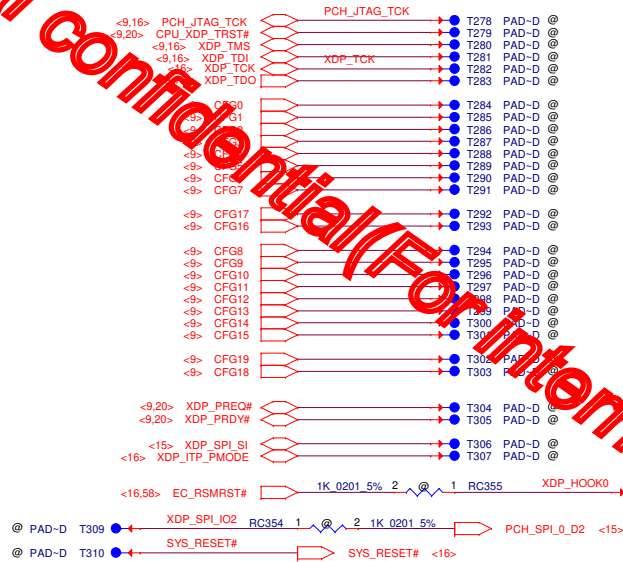
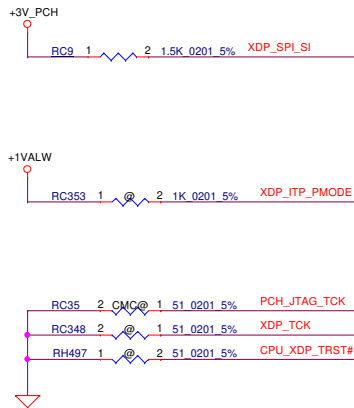
CPU R3:

CPU(Q-SPEC):

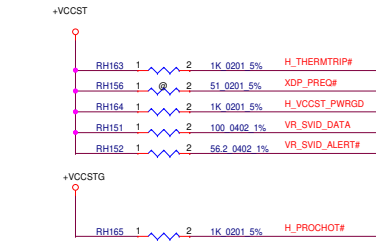
CPU(8C):

Net : EDP_RCOMP
Trace Width/Space: 15 mil/ 20 mil
Max Trace Length: 600 mil

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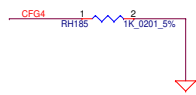
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										LA-J521P	
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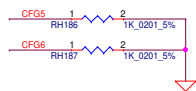
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



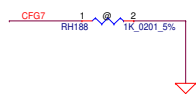
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port ★ 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) ★ 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

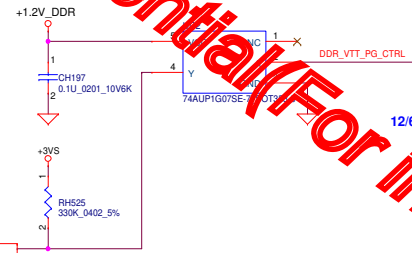


PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



<91,95> VR_SVID_ALERT#
<91,95> VR_SVID_CLK
<91,95> VR_SVID_DATA
<44,58,82,85,85,91> H_PROCHOT#

<58,78> H_VCCST_PWRGD
<16> H_CPU_PWRGD
<14> PLTRST_CPU#
<14> H_PM_SYNC
<14> H_PM_DOWN
<14,58> H_PEG
<14> H_THERMTRIP#
<14> PROC_DETECT#



<15> PCH_CPU_BCLK_P
<15> PCH_CPU_BCLK_N
<15> PCH_CPU_P0BCLK_P
<15> PCH_CPU_P0BCLK_N
<15> CPU_24MHZ_P
<15> CPU_24MHZ_N

VR_SVID_ALERT# RH153 1 2 VR_SVID_ALERT#_R BH431
VR_SVID_DATA RH154 1 2 499 0402 1% BH432
H_PROCHOT# RH155 1 2 499 0402 1% BH433
DDR_VTT_PG_CTRL BT13

H_VCCST_PWRGD RH154 1 2 60.4 0402 1% H13
H_CPU_PWRGD BH31
PLTRST_CPU# BH32
H_PM_SYNC BH33
H_PM_DOWN BH34
H_THERMTRIP# BT34
PROC_DETECT# BT31

VR_SVID_ALERT# RH153 1 2 VR_SVID_ALERT#_R BH431
VR_SVID_DATA RH154 1 2 499 0402 1% BH432
H_PROCHOT# RH155 1 2 499 0402 1% BH433
DDR_VTT_PG_CTRL BT13

+VCCSTG

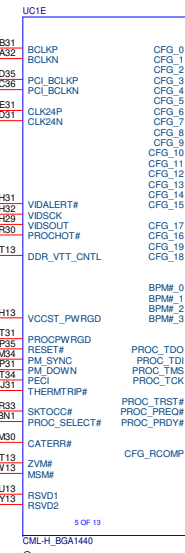
RH153 1 2 0.2 0201 5% PROC_SELECT#
RE716 1 2 0.2 0201 5% PROC_SELECT#
RC693 1 2 51 0201 5% H_CATERR#
BM30

12/6 DVT2 Modify

CH193 1 2 100P 0201 25V8J
ESD@

CH194 1 2 0.1U 0201 10V6K
ESD@

CH195 1 2 0.1U 0201 10V6K
ESD@



CFG_0 BN25
CFG_1 BN27
CFG_2 BN28
CFG_3 BN29
CFG_4 BN30
CFG_5 BT20
CFG_6 BP20
CFG_7 BR23
CFG_8 BR22
CFG_9 BT22
CFG_10 BT23
CFG_11 BM19
CFG_12 BR19
CFG_13 BR19
CFG_14 BT19
CFG_15

BN25
BN27
BN28
BN29
BN30
BT20
BP20
BR23
BR22
BT22
BM19
BR19
BR19
BT19

CFG0 <7>
CFG1 <7>
CFG2 <7>
CFG3 <7>
CFG4 <7>
CFG5 <7>
CFG6 <7>
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CFG14 <7>
CFG15 <7>

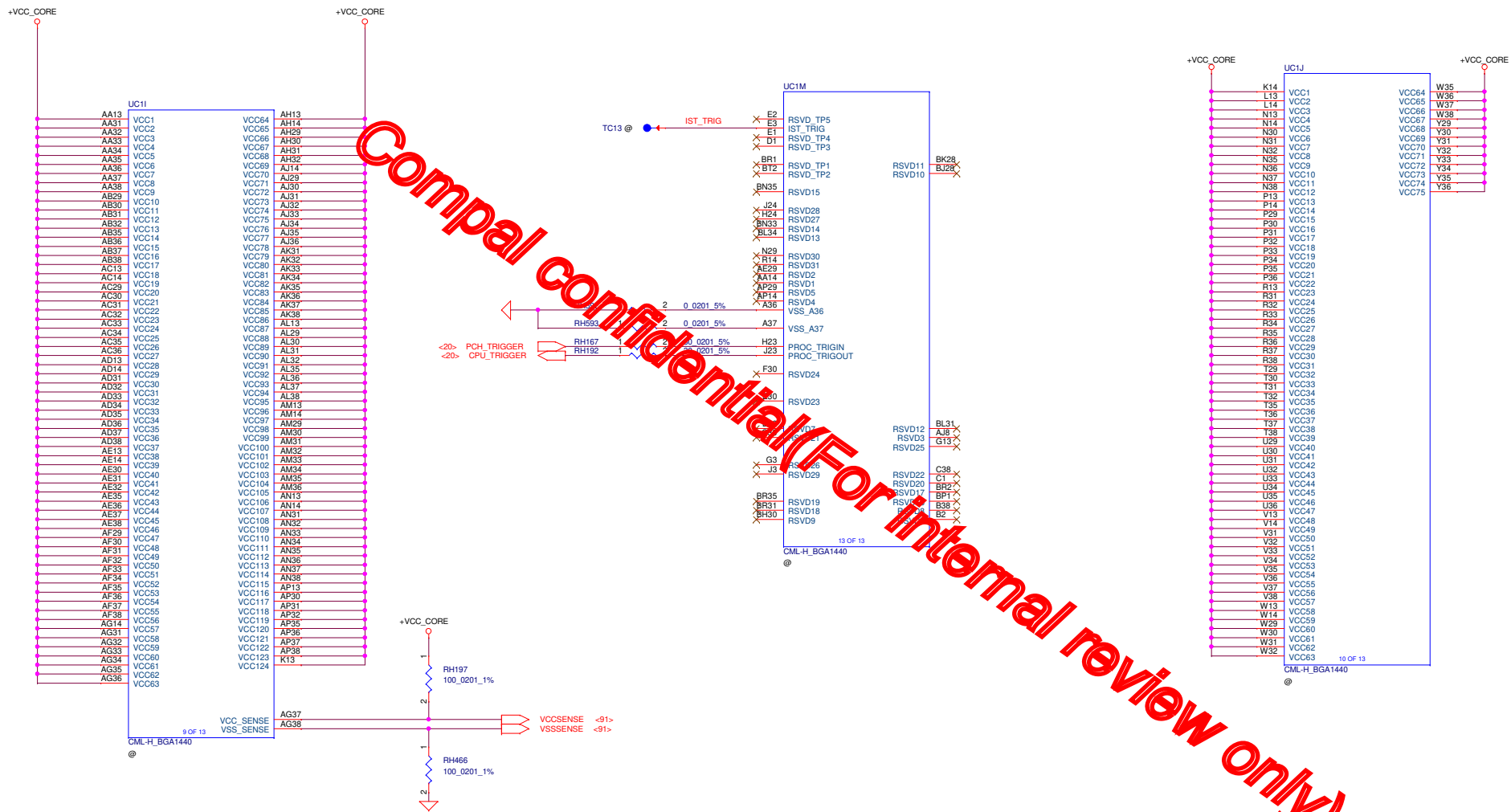
BT28 XDP_TDO
BL32 XDP_TDI
BP28 XDP_TMS
BR28 XDP_TCK
BP30 CPU_XDP_TRST#
BL30 XDP_PREQ#
BP27 XDP_PRTY#

XDP_TDO <7,16>
XDP_TDI <7,16>
XDP_TMS <7,16>
XDP_TCK <7,16>
CPU_XDP_TRST# <7,20>
XDP_PREQ# <7,20>
XDP_PRTY# <7,20>

CFG_RCOMP BT25

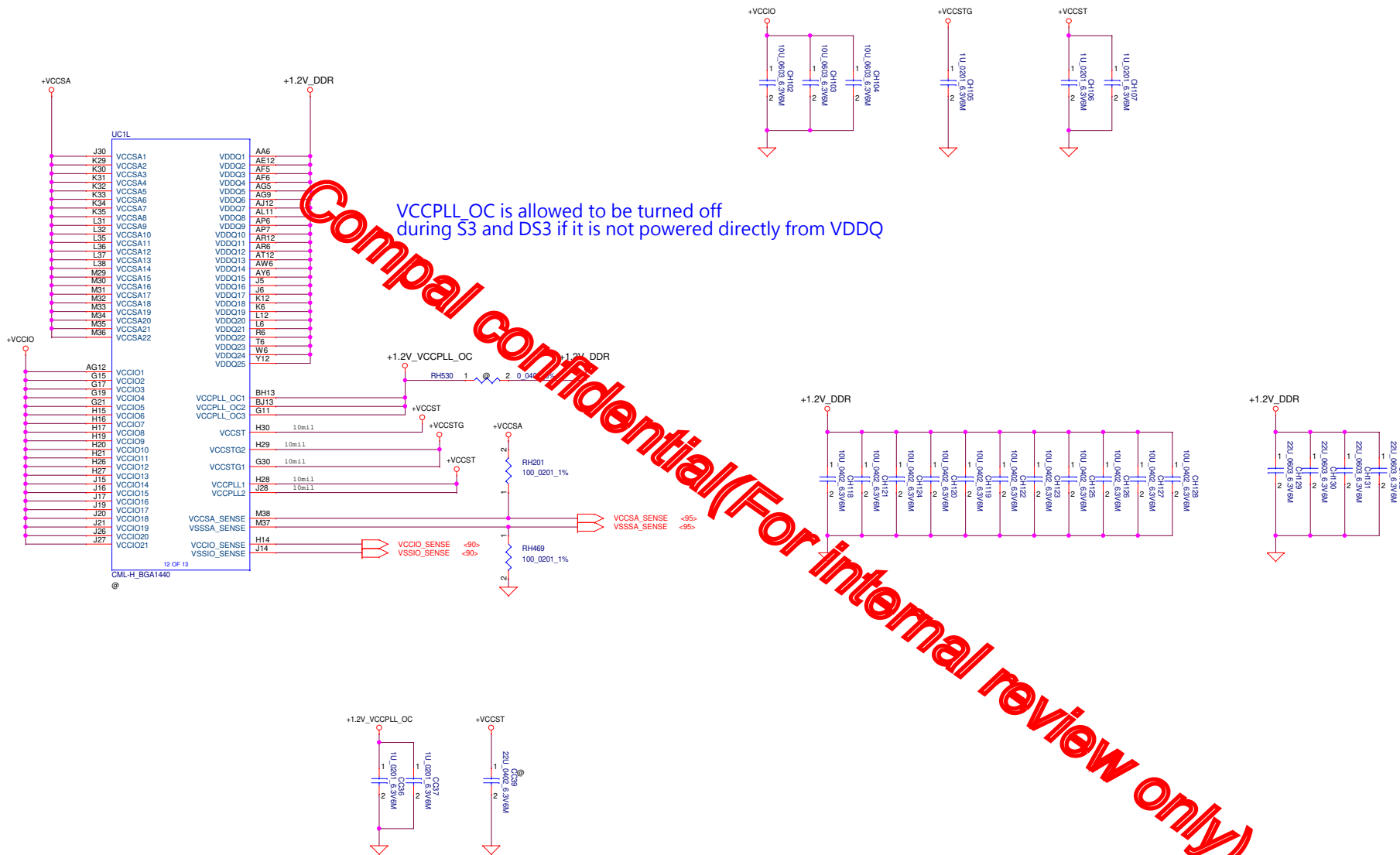
Net: CFG_RCOMP
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

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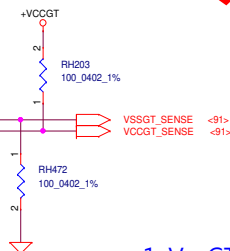
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										Size Document Number	
										LA-J521P	
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1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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UC1F			UC1G			UC1H		
A10	VSS_1	VSS_82	AW5	VSS_163	VSS_244	BN4	VSS_325	VSS_409
A12	VSS_2	VSS_83	AY12	VSS_164	VSS_245	BN7	VSS_326	VSS_410
A16	VSS_3	VSS_84	AY33	VSS_165	VSS_246	BP12	VSS_327	VSS_411
A18	VSS_4	VSS_85	AY34	VSS_166	VSS_247	BP14	VSS_328	VSS_412
A20	VSS_5	VSS_86	BA9	VSS_167	VSS_248	BP18	VSS_329	VSS_413
A22	VSS_6	VSS_87	BA10	VSS_168	VSS_249	BP21	VSS_330	VSS_414
A24	VSS_7	VSS_88	BA11	VSS_169	VSS_250	BP24	VSS_331	VSS_415
A26	VSS_8	VSS_89	BA12	VSS_170	VSS_251	BP25	VSS_332	VSS_416
A28	VSS_9	VSS_90	BA17	VSS_171	VSS_252	BP26	VSS_333	VSS_417
A30	VSS_10	VSS_91	BA38	VSS_172	VSS_253	BP29	VSS_334	VSS_418
A6	VSS_11	VSS_92	BA6	VSS_173	VSS_254	BP33	VSS_335	VSS_419
A9	VSS_12	VSS_93	BA7	VSS_174	VSS_255	BP34	VSS_336	VSS_420
AA12	VSS_13	VSS_94	BA8	VSS_175	VSS_256	BP7	VSS_337	VSS_421
AA29	VSS_14	VSS_95	BA9	VSS_176	VSS_257	BP12	VSS_338	VSS_422
AA30	VSS_15	VSS_96	BB1	VSS_177	VSS_258	BP14	VSS_339	VSS_423
AB33	VSS_16	VSS_97	BB2	VSS_178	VSS_259	BR21	VSS_340	VSS_424
AB34	VSS_17	VSS_98	BB29	VSS_179	VSS_260	BR24	VSS_341	VSS_425
AB8	VSS_18	VSS_99	BB3	VSS_180	VSS_261	BR25	VSS_342	VSS_426
AC1	VSS_19	VSS_100	BB30	VSS_181	VSS_262	BR26	VSS_343	VSS_427
AC12	VSS_20	VSS_101	BB4	VSS_182	VSS_263	BR29	VSS_344	VSS_428
AC2	VSS_21	VSS_102	BB5	VSS_183	VSS_264	BR34	VSS_345	VSS_429
AC3	VSS_22	VSS_103	BB6	VSS_184	VSS_265	BR36	VSS_346	VSS_430
AC37	VSS_23	VSS_104	BC12	VSS_185	VSS_266	BR7	VSS_347	VSS_431
AC38	VSS_24	VSS_105	BC13	VSS_186	VSS_267	BT12	VSS_348	VSS_432
AC4	VSS_25	VSS_106	BC14	VSS_187	VSS_268	BT14	VSS_349	VSS_433
AC5	VSS_26	VSS_107	BC33	VSS_188	VSS_269	BT18	VSS_350	VSS_434
AC6	VSS_27	VSS_108	BC34	VSS_189	VSS_270	BT21	VSS_351	VSS_435
AD10	VSS_28	VSS_109	BC6	VSS_190	VSS_271	BT24	VSS_352	VSS_436
AD11	VSS_29	VSS_110	BC9	VSS_191	VSS_272	BT26	VSS_353	VSS_437
AD12	VSS_30	VSS_111	BD11	VSS_192	VSS_273	BT29	VSS_354	VSS_438
AD29	VSS_31	VSS_112	BD12	VSS_193	VSS_274	BT32	VSS_355	VSS_439
AD30	VSS_32	VSS_113	BE1	VSS_194	VSS_275	BT5	VSS_356	VSS_440
AD6	VSS_33	VSS_114	BE2	VSS_195	VSS_276	C11	VSS_357	VSS_441
AD8	VSS_34	VSS_115	BE29	VSS_196	VSS_277	C13	VSS_358	VSS_442
AD9	VSS_35	VSS_116	BD9	VSS_197	VSS_278	C15	VSS_359	VSS_443
AE33	VSS_36	VSS_117	BE1	VSS_198	VSS_279	C17	VSS_360	VSS_444
AE34	VSS_37	VSS_118	BE1	VSS_199	VSS_280	C19	VSS_361	VSS_445
AE6	VSS_38	VSS_119	BE2	VSS_200	VSS_281	C21	VSS_362	VSS_446
AF1	VSS_39	VSS_120	BE29	VSS_201	VSS_282	C23	VSS_363	VSS_447
AF12	VSS_40	VSS_121	BE3	VSS_202	VSS_283	C25	VSS_364	VSS_448
AF13	VSS_41	VSS_122	BE30	VSS_203	VSS_284	C27	VSS_365	VSS_449
AF14	VSS_42	VSS_123	BE4	VSS_204	VSS_285	C29	VSS_366	VSS_450
AF2	VSS_43	VSS_124	BE5	VSS_205	VSS_286	C31	VSS_367	VSS_451
AF3	VSS_44	VSS_125	BE6	VSS_206	VSS_287	C37	VSS_368	VSS_452
AF4	VSS_45	VSS_126	BF12	VSS_207	VSS_288	C5	VSS_369	VSS_453
AG10	VSS_46	VSS_127	BF33	VSS_208	VSS_289	C8	VSS_370	VSS_454
AG11	VSS_47	VSS_128	BF34	VSS_209	VSS_290	C9	VSS_371	VSS_455
AG13	VSS_48	VSS_129	BF6	VSS_210	VSS_291	D10	VSS_372	VSS_456
AG29	VSS_49	VSS_130	BG12	VSS_211	VSS_292	D12	VSS_373	VSS_457
AG30	VSS_50	VSS_131	BG13	VSS_212	VSS_293	D14	VSS_374	VSS_458
AG6	VSS_51	VSS_132	BG14	VSS_213	VSS_294	D16	VSS_375	VSS_459
AG7	VSS_52	VSS_133	BG37	VSS_214	VSS_295	D6	VSS_376	VSS_460
AG8	VSS_53	VSS_134	BG38	VSS_215	VSS_296	D8	VSS_377	VSS_461
AH12	VSS_54	VSS_135	BG6	VSS_216	VSS_297	D9	VSS_378	VSS_462
AH33	VSS_55	VSS_136	BH1	VSS_217	VSS_298	D25	VSS_379	VSS_463
AH34	VSS_56	VSS_137	BH10	VSS_218	VSS_299	D28	VSS_380	VSS_464
AH35	VSS_57	VSS_138	BH11	VSS_219	VSS_300	D3	VSS_381	VSS_465
AH36	VSS_58	VSS_139	BH12	VSS_220	VSS_301	D33	VSS_382	VSS_466
AH6	VSS_59	VSS_140	BH14	VSS_221	VSS_302	D30	VSS_383	VSS_467
AJ1	VSS_60	VSS_141	BH2	VSS_222	VSS_303	D33	VSS_384	VSS_468
AJ13	VSS_61	VSS_142	BH3	VSS_223	VSS_304	D6	VSS_385	VSS_469
AJ2	VSS_62	VSS_143	BH4	VSS_224	VSS_305	D9	VSS_386	VSS_470
AJ3	VSS_63	VSS_144	BH5	VSS_225	VSS_306	E34	VSS_387	VSS_471
AJ37	VSS_64	VSS_145	BH6	VSS_226	VSS_307	E35	VSS_388	VSS_472
AJ38	VSS_65	VSS_146	BH7	VSS_227	VSS_308	E38	VSS_389	VSS_473
AJ4	VSS_66	VSS_147	BH8	VSS_228	VSS_309	E4	VSS_390	VSS_474
AJ5	VSS_67	VSS_148	BH9	VSS_229	VSS_310	E9	VSS_391	VSS_475
AJ6	VSS_68	VSS_149	I2	VSS_230	VSS_311	N3	VSS_392	VSS_476
W4	VSS_69	VSS_150	I3	VSS_231	VSS_312	N33	VSS_393	VSS_477
W5	VSS_70	VSS_151	I4	VSS_232	VSS_313	N34	VSS_394	VSS_478
Y10	VSS_71	VSS_152	I5	VSS_233	VSS_314	N4	VSS_395	VSS_479
Y11	VSS_72	VSS_153	I6	VSS_234	VSS_315	N5	VSS_396	VSS_480
Y13	VSS_73	VSS_154	I7	VSS_235	VSS_316	N6	VSS_397	VSS_481
Y14	VSS_74	VSS_155	I8	VSS_236	VSS_317	N7	VSS_398	VSS_482
Y37	VSS_75	VSS_156	I9	VSS_237	VSS_318	N8	VSS_399	VSS_483
Y8	VSS_76	VSS_157	I10	VSS_238	VSS_319	N9	VSS_400	VSS_484
Y9	VSS_77	VSS_158	I11	VSS_239	VSS_320	P12	VSS_401	VSS_485
Y9	VSS_78	VSS_159	I12	VSS_240	VSS_321	P37	VSS_402	VSS_486
AK29	VSS_79	VSS_160	I13	VSS_241	VSS_322	M14	VSS_403	VSS_487
AK30	VSS_80	VSS_161	I14	VSS_242	VSS_323	M6	VSS_404	VSS_488
AK30	VSS_81	VSS_162	I14	VSS_243	VSS_324	N1	VSS_405	VSS_489

CML-H_BGA1440
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CML-H_BGA1440
8 OF 13

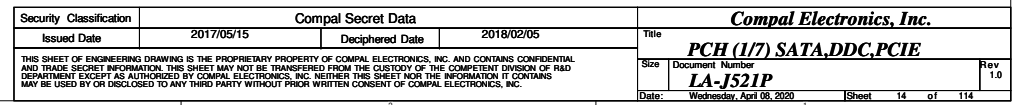
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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	CPU(7/7) VSS
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				Sheet	13 of 114
				Rev	1.0
				LA-J521P	

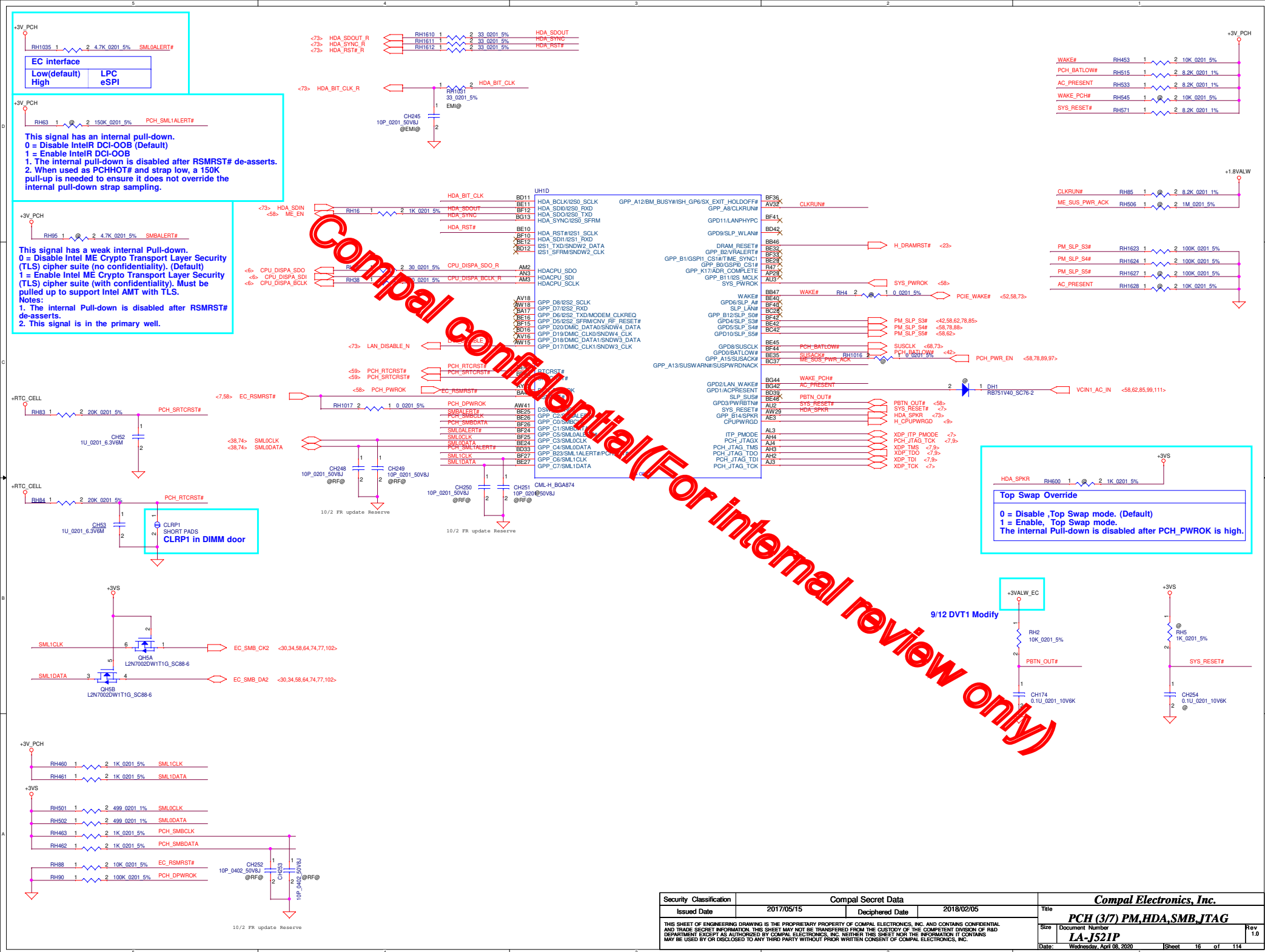
U#1

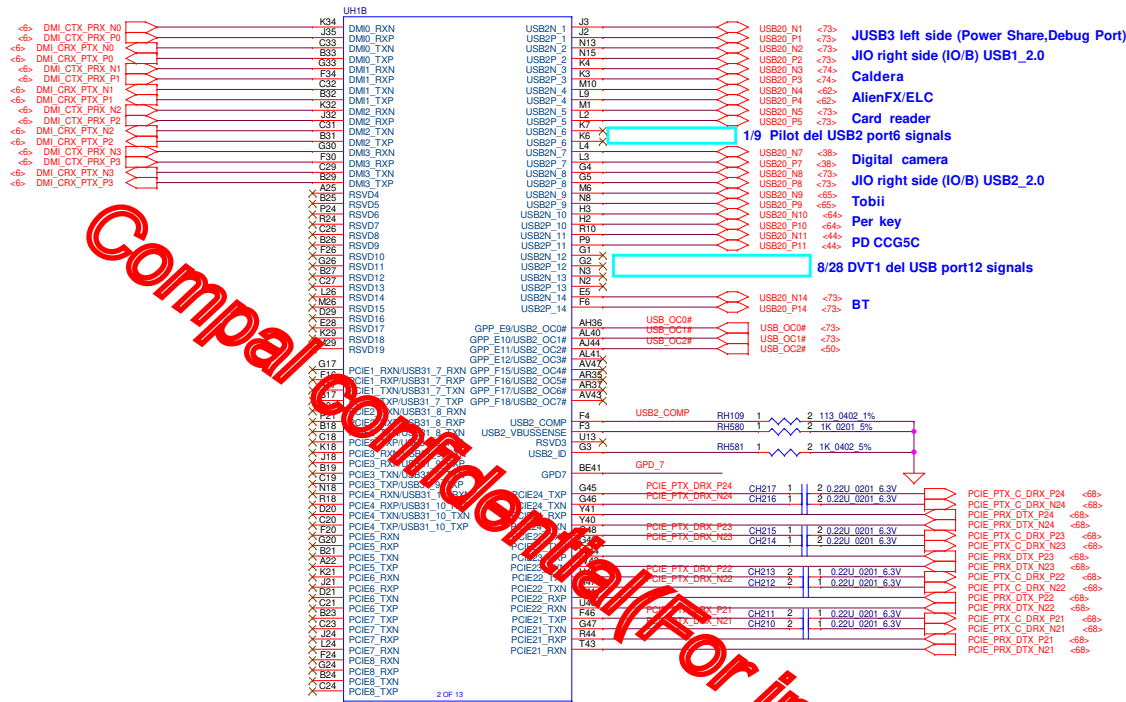
FH82HM470 SRJAU A0 FCBGA PCH-H A31!
SA0000DDP4L
PCH@

U#1

FH82HM470 SRJAU A0 FCBGA 874P PCH-H
SA0000DDP3L
PCH1@







Card reader

JUSB1

JUSB2

Caldera

JIO left JUSB3

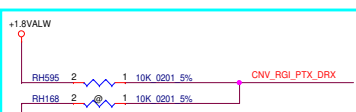
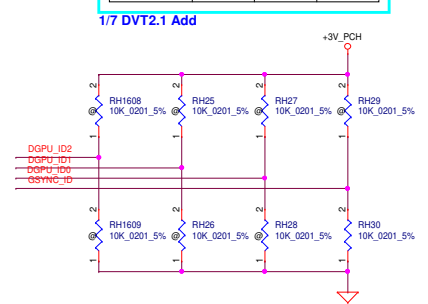
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2017/05/15		Title	
Deciphered Date		2018/02/05		PCH (4/7) DMI,PCIE,USB,LPC	
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Pinout diagram for the Raspberry Pi 4 Model B, showing the 40-pin header with pin numbers and functions. The diagram is color-coded: blue for power and ground, green for UART, red for I2C, and purple for SPI. A +3V5 pin is shown on the left. The functions listed on the right include BT_OFF#, WL_OFF#, EC_SCK#, UART_2_TXD, UART_2_RXD, and SD_WIF#.

Pin	Function
1	3V3
2	5V
3	GND
4	5V
5	GND
6	GPIO0
7	GPIO1
8	GPIO2
9	GPIO3
10	GPIO4
11	GPIO5
12	GPIO6
13	GPIO7
14	GPIO8
15	GPIO9
16	GPIO10
17	GPIO11
18	GPIO12
19	GPIO13
20	GPIO14
21	GPIO15
22	GPIO16
23	GPIO17
24	GPIO18
25	GPIO19
26	GPIO20
27	GPIO21
28	GPIO22
29	GPIO23
30	GPIO24
31	GPIO25
32	GPIO26
33	GPIO27
34	GPIO28
35	GPIO29
36	GPIO30
37	GPIO31
38	GPIO32
39	GPIO33
40	GPIO34

N18P-G62	N18PQ0@ RH1608 10K_0201_5%	N18PQ0@ RH26 10K_0201_5%	N18PQ0@ RH27 10K_0201_5%
N18E-G3	N18EG3@ RH1608 10K_0201_5%	N18EG3@ RH27 10K_0201_5%	N18EG3@ RH28 10K_0201_5%
N18E-G2	N18EG2@ RH1608 10K_0201_5%	N18EG2@ RH26 10K_0201_5%	N18EG2@ RH28 10K_0201_5%
N18E-G1	N18EG1@ RH1608 10K_0201_5%	N18EG1@ RH25 10K_0201_5%	N18EG1@ RH2 10K_0201_5%
N18E-G0	N18EG0@ RH1600 10K_0201_5%	N18EG0@ RH25 10K_0201_5%	N18EG0@ RH28 10K_0201_5%
Navi 14 XTM	AMD@ RH1609 10K_0201_5%	AMD@ RH26 10K_0201_5%	AMD@ RH28 10K_0201_5%
N18E-G1-B	N18EG1B@ RH1609 10K_0201_5%	N18EG1B@ RH26 10K_0201_5%	N18EG1B@ RH28 10K_0201_5%

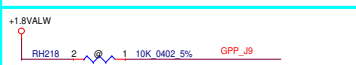
GPU_ID	N18_ID2 (BF14)	N18_ID1 (AR18)	N18_ID0 (BF17)
N18E-G3	H	L	H
N18E-G2	H	L	L
N18E-G1	L	H	H
N18E-G0	L	H	L
N18P-G62	L	L	H
Navi 14 XTM	L	L	L
N18E-G1B	H	H	L



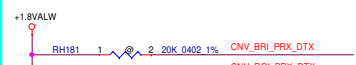
M.2 CNV Mode Select	
<p>An external pull-up or pull-down is required. 0 = Integrated CNVI enable. 1 = Integrated CNVI disable. Pulled down by CRF CNVI RGL_DT pin</p>	



This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

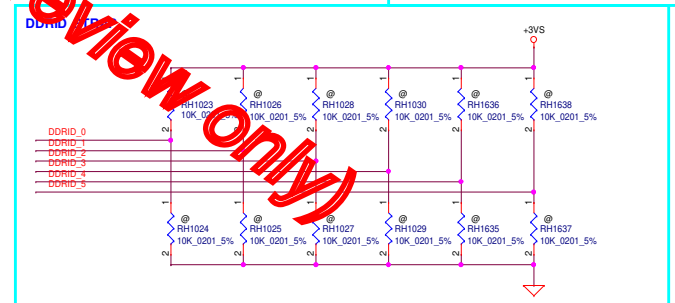
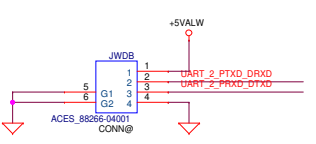


The signal has a weak internal pull-down
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin
strap must be 1 for the proper functionality
of the SPI (Flash) I/Os



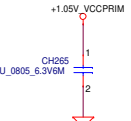
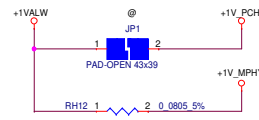
571391_CFL_H_PDG_Rev0p71

For BIOS UART debug

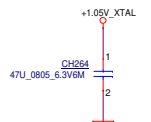


Vendor	DDRID_0	DDRID_1	Vendor	DDRID_2	DDRID_3	Vendor	DDRID_4	DDRID_5
Samsung	L	L	8G	L	L	8G	L(1st die) H(2nd die)	RSVD
Hynix	H	L	16G	H	L	16G		RSVD
Micron	L	H	32G	L	H	32G		RSVD

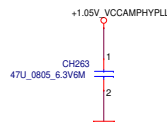
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			Size	Document Number
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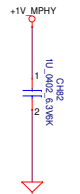
Close to E1, D1



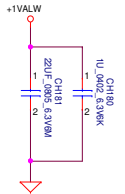
Close to P2, P3



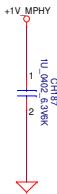
Close to C49, D49, E49



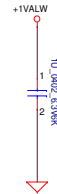
Close to B1,B2,B3,C1,C2



Close to U26,U29V25,V27,V28,V30,V31



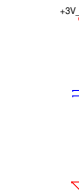
Close to C49,D49,E49



Close to AF31,AG31,AD31,AA22,AA23
,AB20,AB22,AB23,AB27,AB28,AB30
,AD20,AD23,AD27,AD28,AD30,AF23
,AF27,AF30,AE17



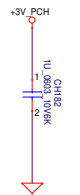
Close to AG19,AG20
,AR15,AN15,BB11



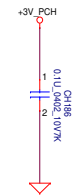
Close to AE35,AE36



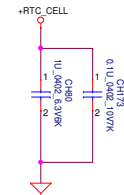
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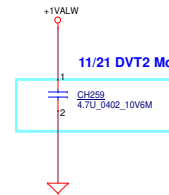
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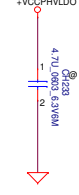
Close to BE48,BE49



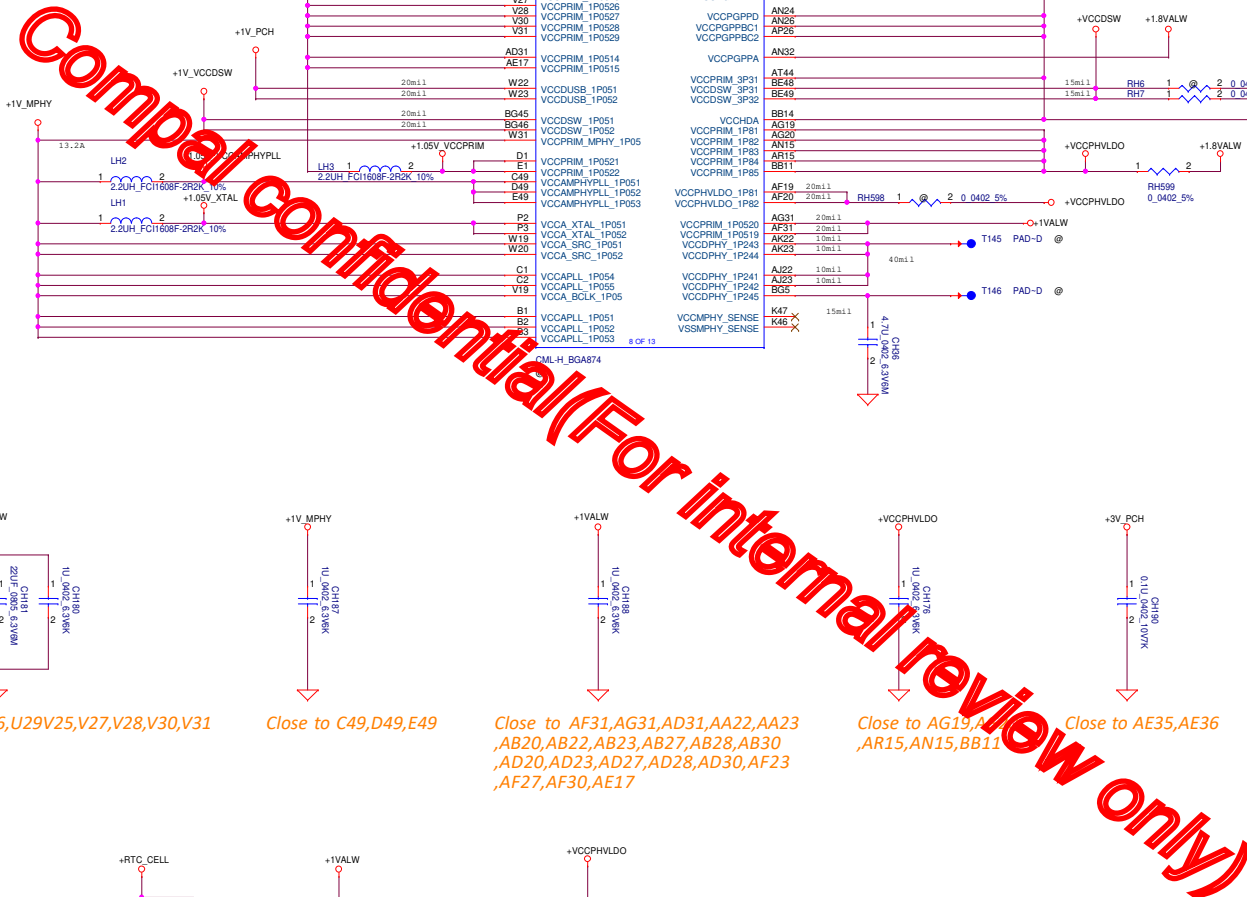
Close to BC49,BD49



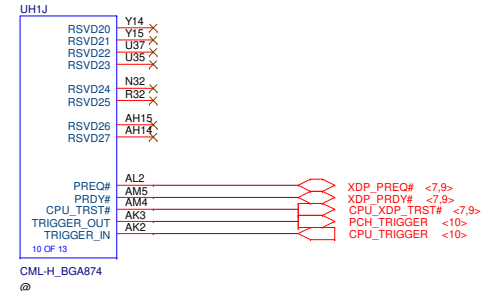
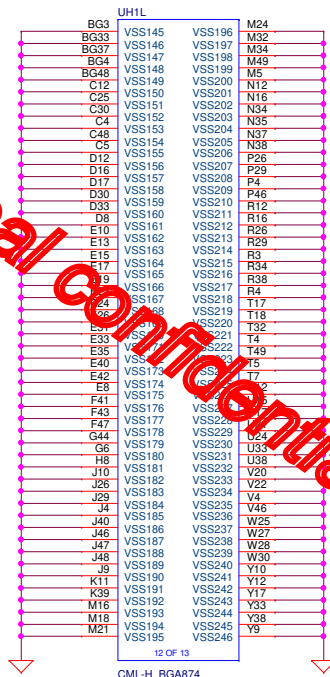
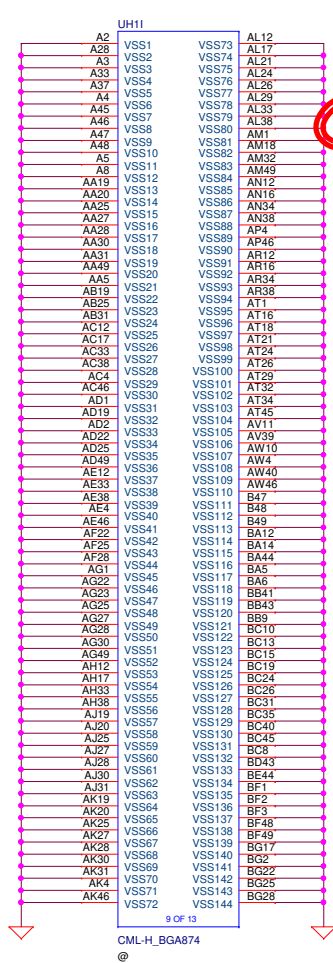
Close to E1,D1



Close to AG19,AG20
,AR15,AN15,BB11



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				Size Document Number
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				Rev 1.0
				Date: Wednesday, April 08, 2020
				Sheet 19 of 114



VRAM X76:

2223 X76AG0

ALT. GROUP PARTS VRAM 6G MICRON FQ051
X76B231L01

2224 X76AG0

ALT. GROUP PARTS VRAM 6G SAMSUNG FQ051
X76B231L03

2225 X76AG0

ALT. GROUP PARTS VRAM 8G 1.2V MIC FQ051
X76B231L03

2226 X76AG0

ALT. GROUP PARTS VRAM 8G 1.2V SAM FQ051
X76B231L04

2227 X76AG0

ALT. GROUP PARTS 6G MIC FOR G18 FQ051
X76B231L19

2228 X76AG0

ALT. GROUP PARTS 6G SAM FOR G18 FQ051
X76B231L20

8G bit GDDR6(EG0)			
Micron 6G Byte		Samsung 6G Byte	
R1	R3	R1	R3
U011 VMGR1B MT61K256M32JE-14A SA0000BN0L	U015 VMGR1B MT61K256M32JE-14A SA0000BN0L	U011 V56GR1B K4Z80325BC-HC14 SA0000C6L	U015 V56GR1B K4Z80325BC-HC14 SA0000C6L
U012 VMGR1B MT61K256M32JE-14A SA0000BN0L	U016 VMGR1B MT61K256M32JE-14A SA0000BN0L	U012 V56GR1B K4Z80325BC-HC14 SA0000C6L	U016 V56GR1B K4Z80325BC-HC14 SA0000C6L
U013 VMGR1B MT61K256M32JE-14A SA0000BN0L	U017 VMGR1B MT61K256M32JE-14A SA0000BN0L	U013 V56GR1B K4Z80325BC-HC14 SA0000C6L	U017 V56GR1B K4Z80325BC-HC14 SA0000C6L
U014 VMGR1B MT61K256M32JE-14A SA0000BN0L	U018 VMGR1B MT61K256M32JE-14A SA0000BN0L	U014 V56GR1B K4Z80325BC-HC14 SA0000C6L	U018 V56GR1B K4Z80325BC-HC14 SA0000C6L

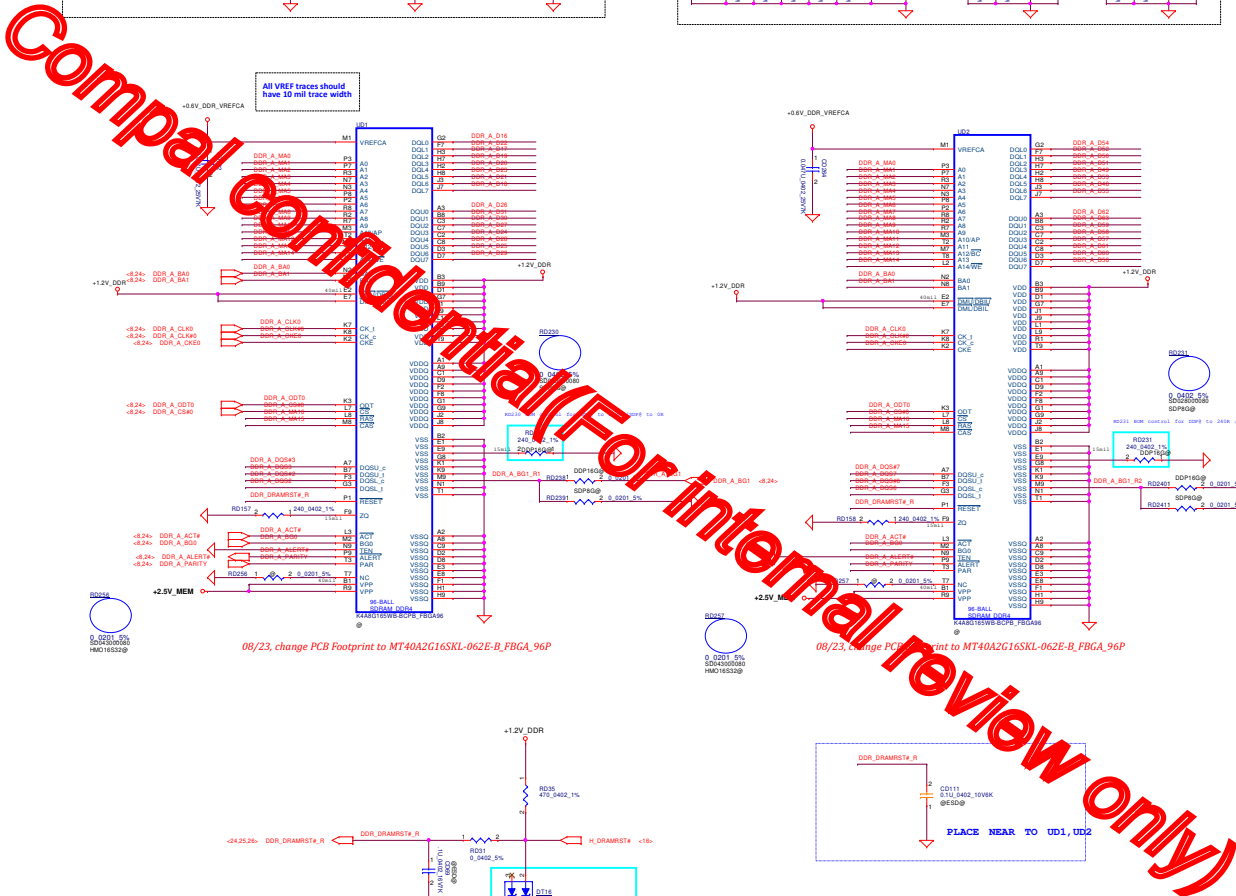
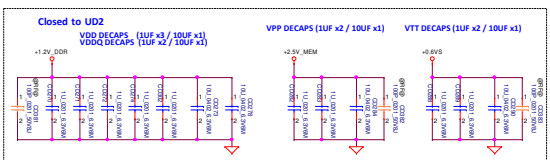
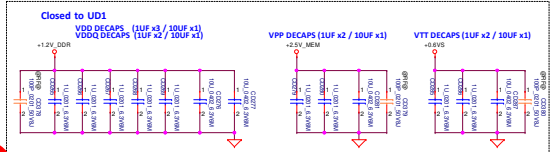
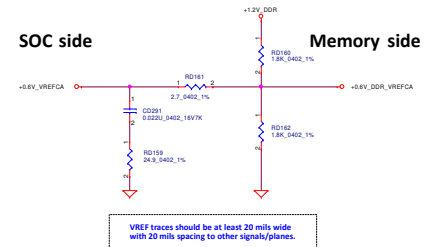
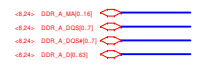
8G bit GDDR6(EG1B)			
Micron 8G Byte		Samsung 8G Byte	
R1	R3	R1	R3
U011 VMGR1B MT61K256M32JE-14A SA0000BN0L	U015 VMGR1B MT61K256M32JE-14A SA0000BN0L	U011 V56GR1B K4Z80325BC-HC14 SA0000C6L	U015 V56GR1B K4Z80325BC-HC14 SA0000C6L
U012 VMGR1B MT61K256M32JE-14A SA0000BN0L	U016 VMGR1B MT61K256M32JE-14A SA0000BN0L	U012 V56GR1B K4Z80325BC-HC14 SA0000C6L	U016 V56GR1B K4Z80325BC-HC14 SA0000C6L
U013 VMGR1B MT61K256M32JE-14A SA0000BN0L	U017 VMGR1B MT61K256M32JE-14A SA0000BN0L	U013 V56GR1B K4Z80325BC-HC14 SA0000C6L	U017 V56GR1B K4Z80325BC-HC14 SA0000C6L
U014 VMGR1B MT61K256M32JE-14A SA0000BN0L	U018 VMGR1B MT61K256M32JE-14A SA0000BN0L	U014 V56GR1B K4Z80325BC-HC14 SA0000C6L	U018 V56GR1B K4Z80325BC-HC14 SA0000C6L

8G bit GDDR6(EG1B)			
Micron 6G Byte		Samsung 6G Byte	
R1	R3	R1	R3
U011 VMGR1B MT61K256M32JE-14A SA0000BN0L	U015 VMGR1B MT61K256M32JE-14A SA0000BN0L	U011 V56GR1B K4Z80325BC-HC14 SA0000C6L	U015 V56GR1B K4Z80325BC-HC14 SA0000C6L
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DDR4 Memory Down_CHA

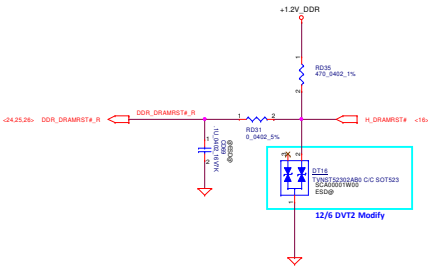
Non-Interleave Memory

DDR4 Memory Down_CHA



08/23, change PCB Footprint to MT40A2G16SKL-062E-B_FPGA_96P

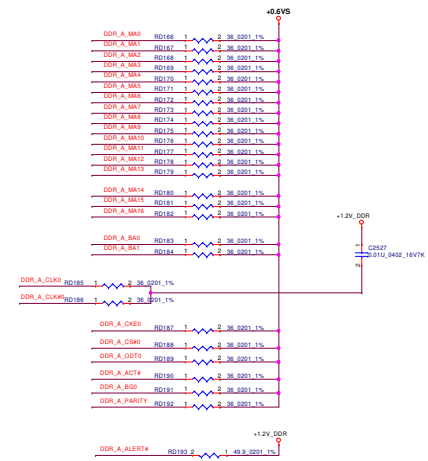
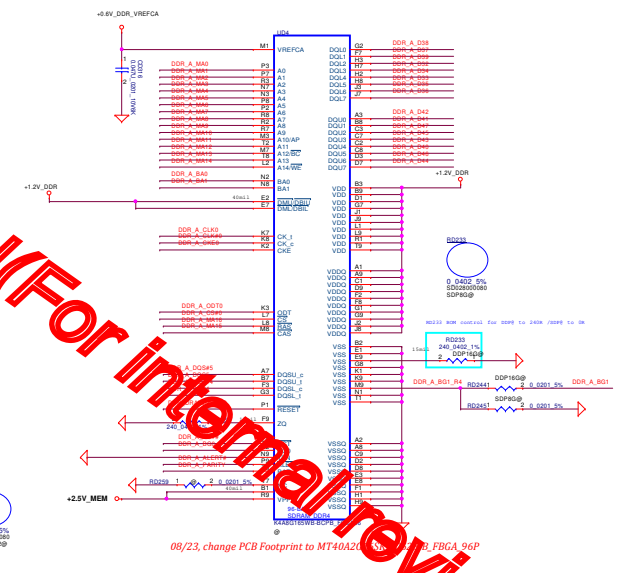
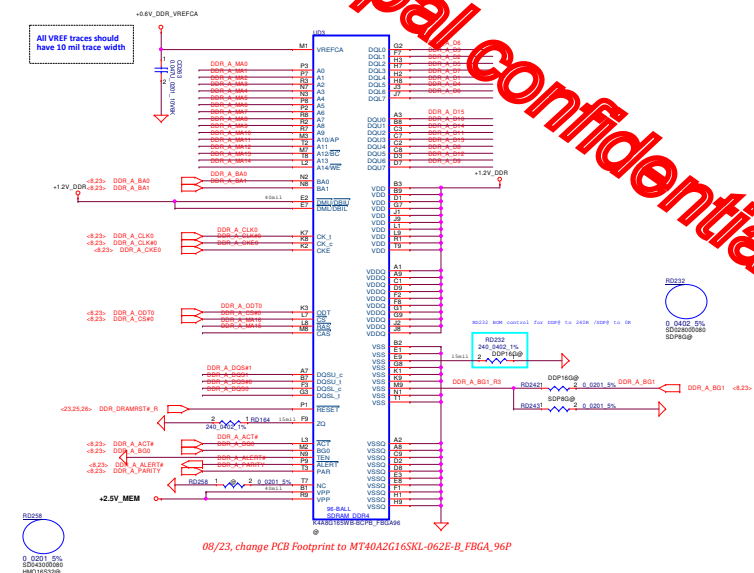
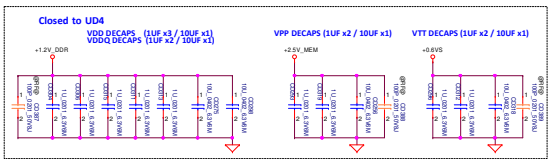
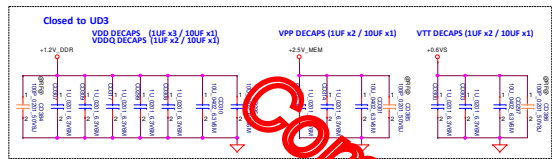
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Security Classification	Compul Secret Data	2018/05/01	2018/05/01
Issued Date	2017/04/07	2018/05/01	2018/05/01
Rev	1.0	1.0	1.0
Rev	1.0	1.0	1.0

DDR4 Memory Down_CHA
Non-Interleave Memory

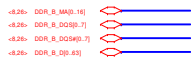
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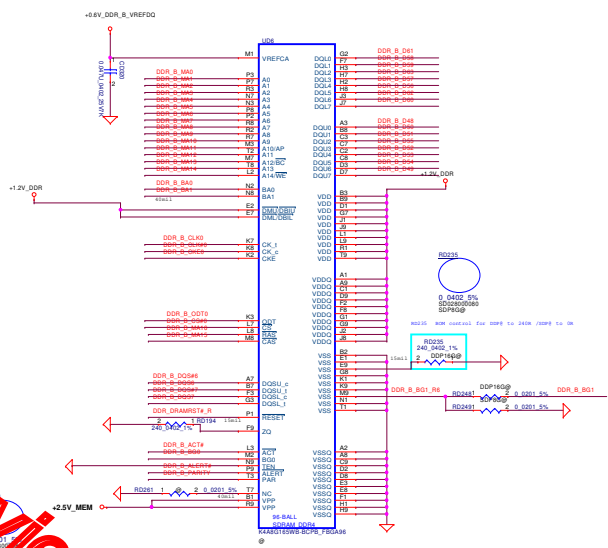
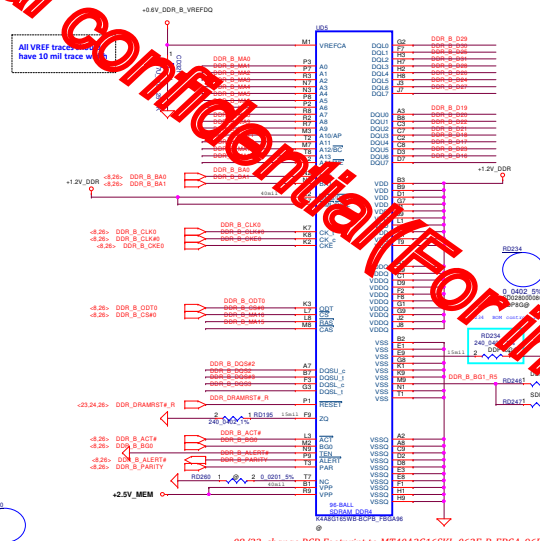
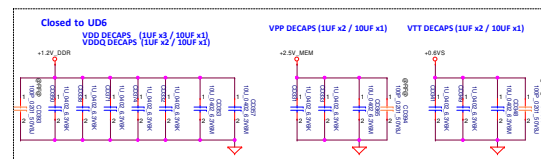
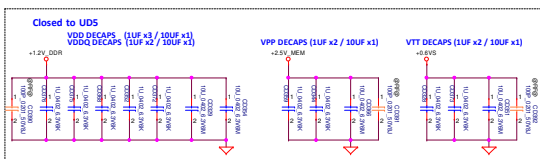
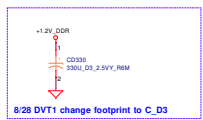
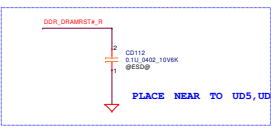
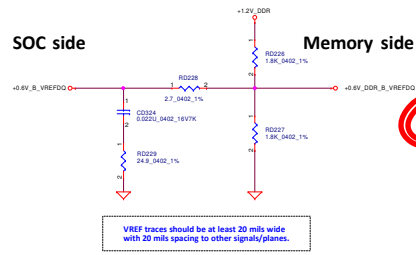
Security Classification	Confidential	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2017/6/27	Designated Date	2016/12/31
View	Designated	View	Designated
Doc No	LA-J521P	Rev	1.0
Print	Wednesday, April 19, 2018	Print	24 of 114

DDR4 Memory Down_CHB

Non-Interleave Memory



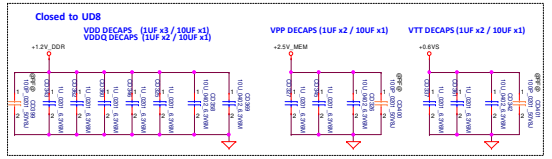
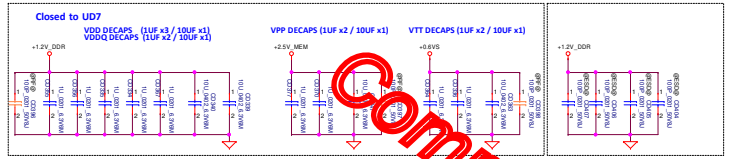
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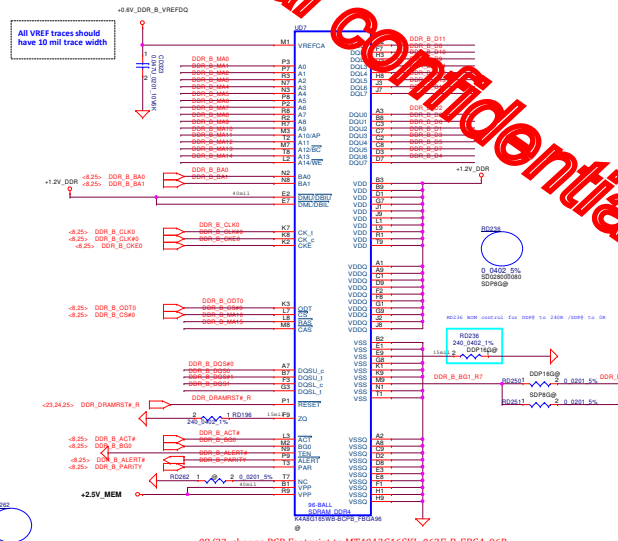
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DRAWN: 2017/04/07				1/4

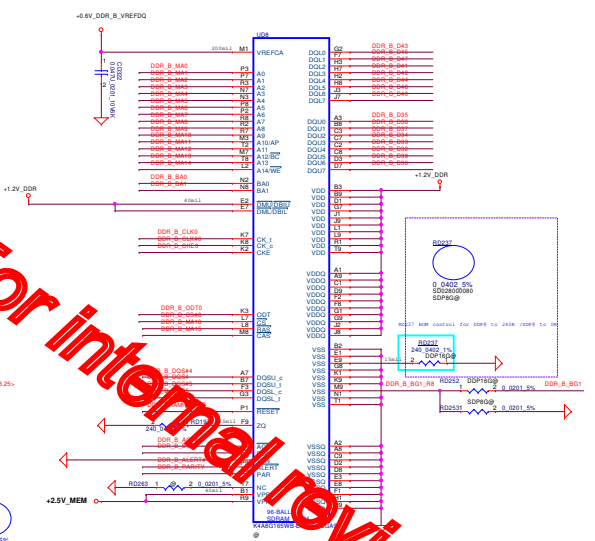
DDR4 Memory Down_CHB
Non-Interleave Memory



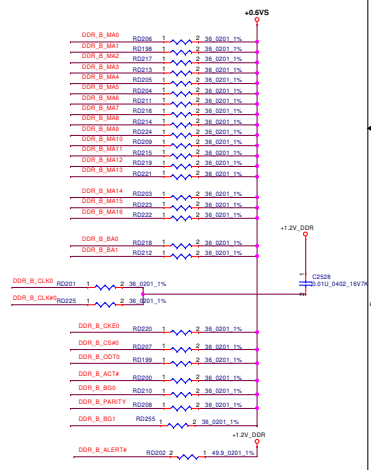
All VREF traces should have 30 mil trace width



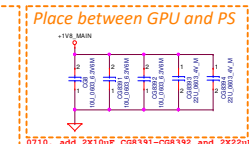
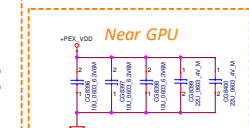
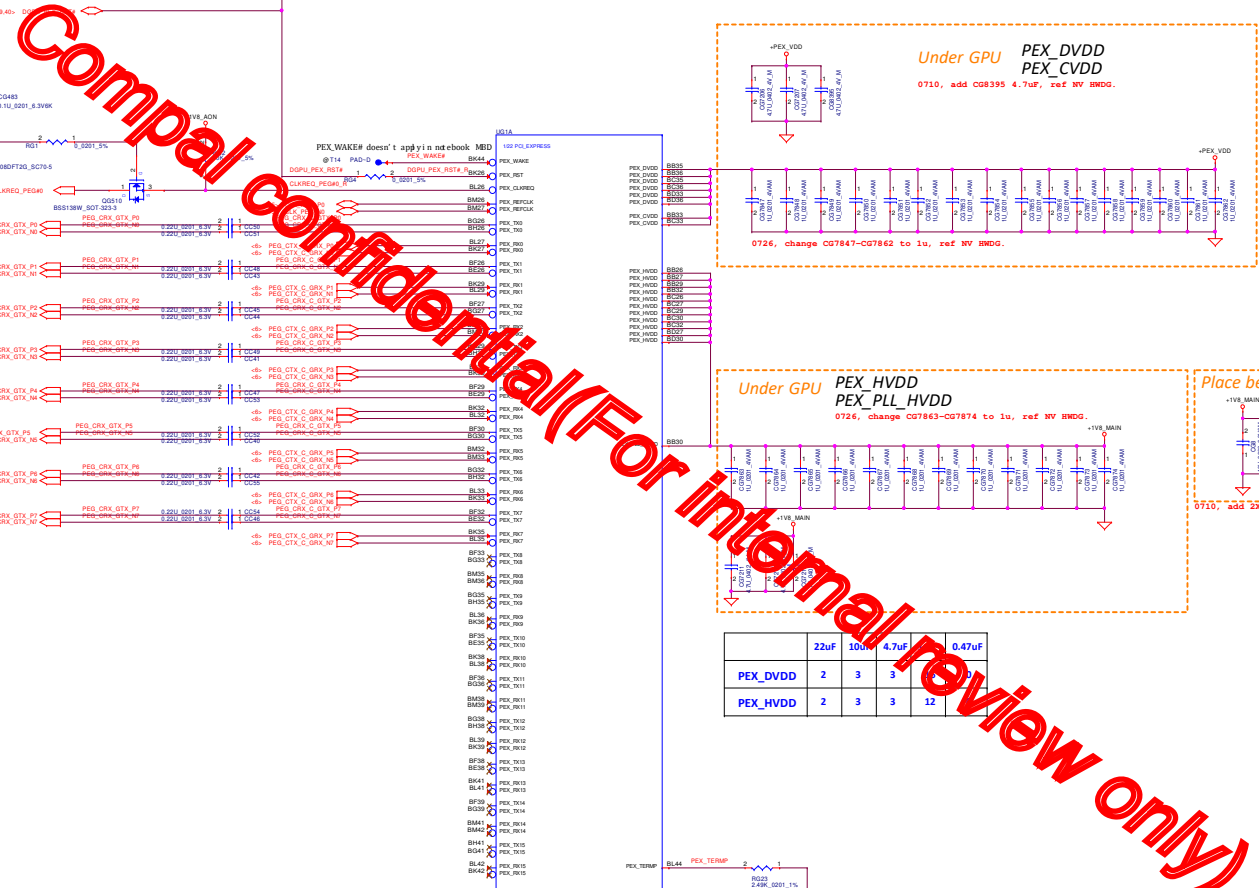
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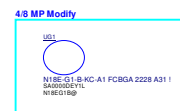
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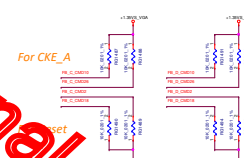
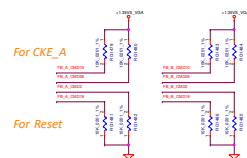
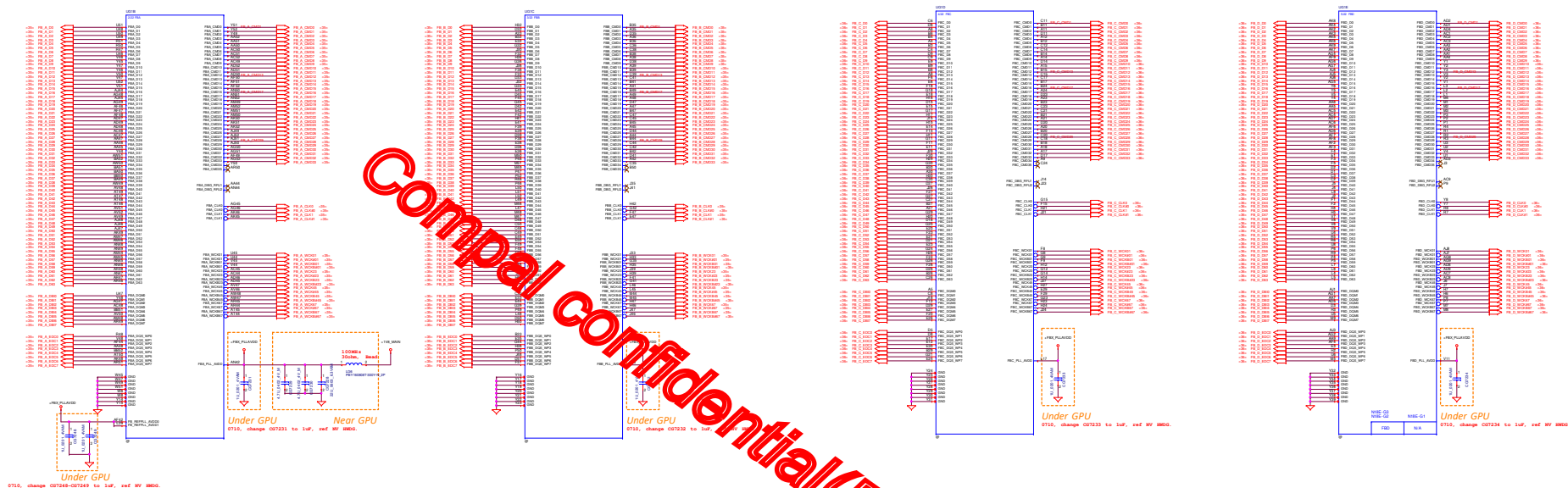


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Designed Date	2016/10/31	LA-J521P
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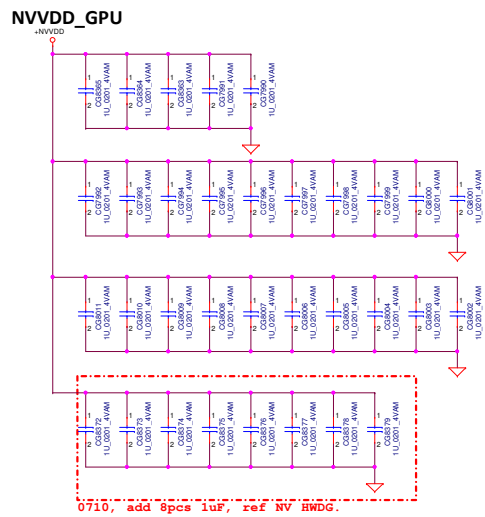
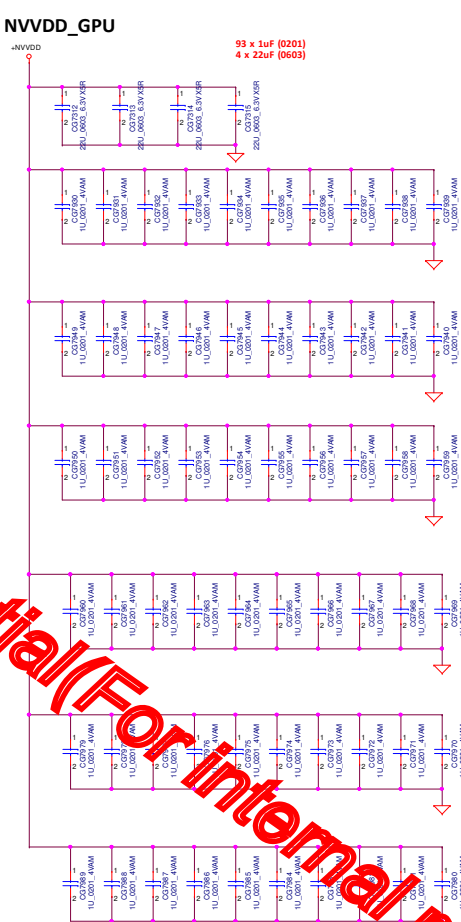
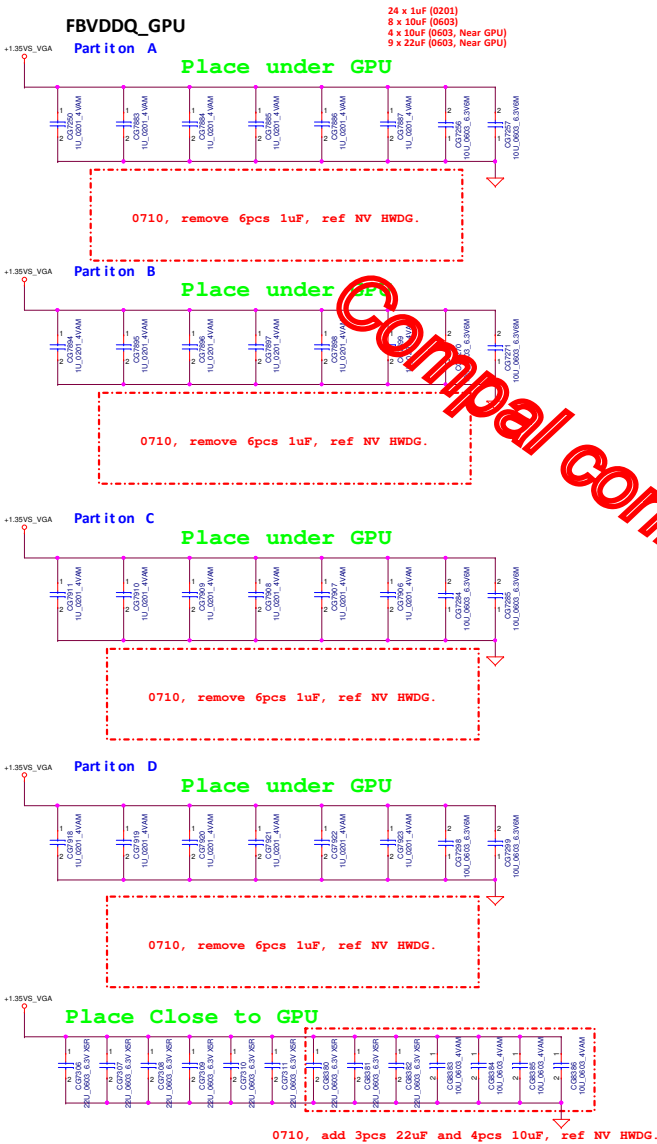


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PEX_HVDD	2	3	3	12





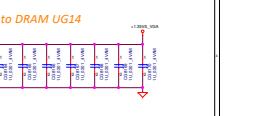
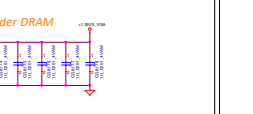
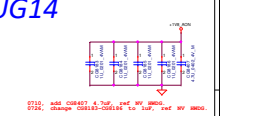
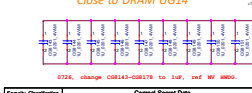
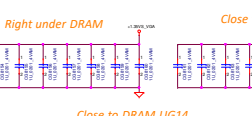
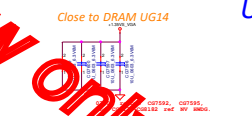
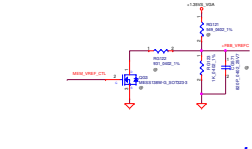
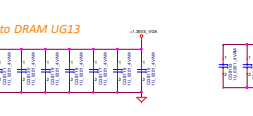
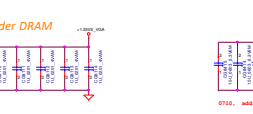
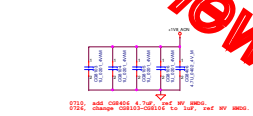
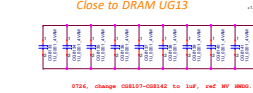
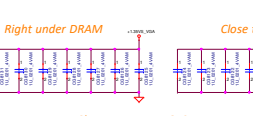
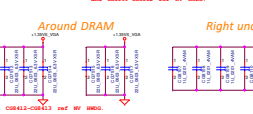
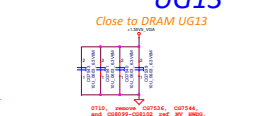
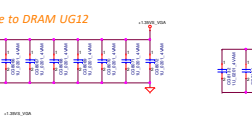
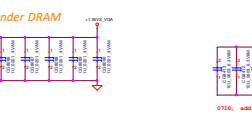
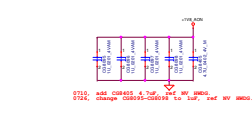
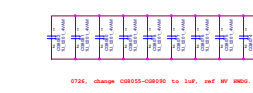
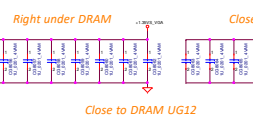
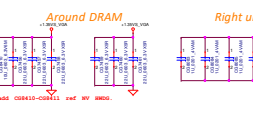
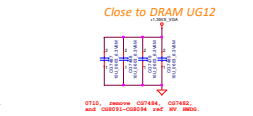
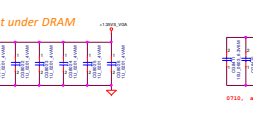
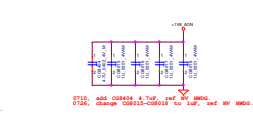
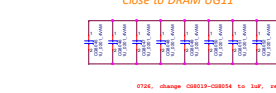
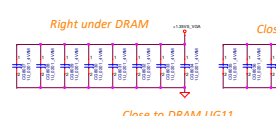
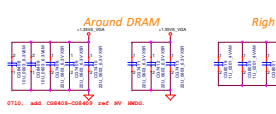
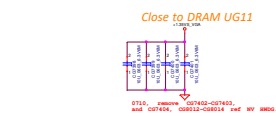
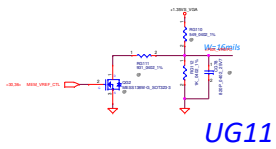
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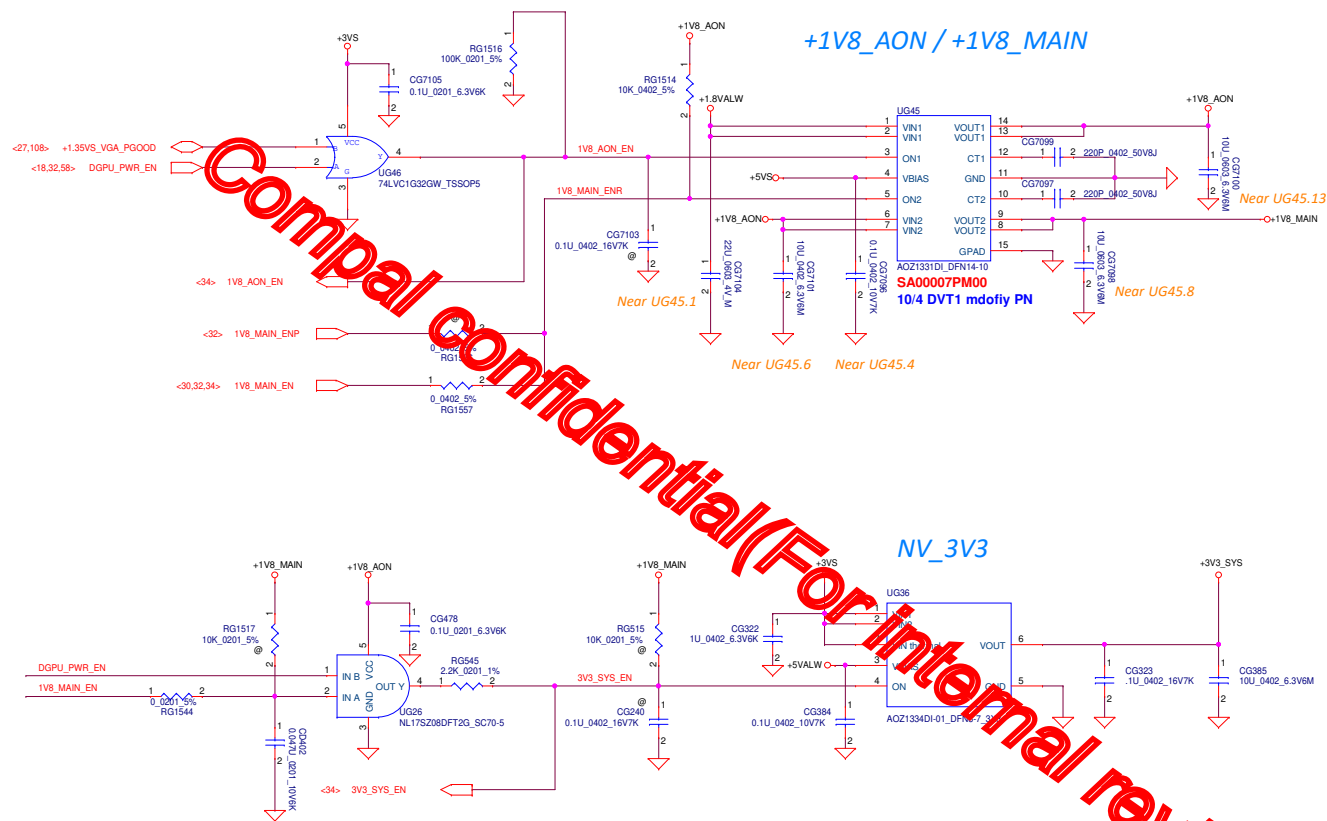


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				Sheet	39 of 114

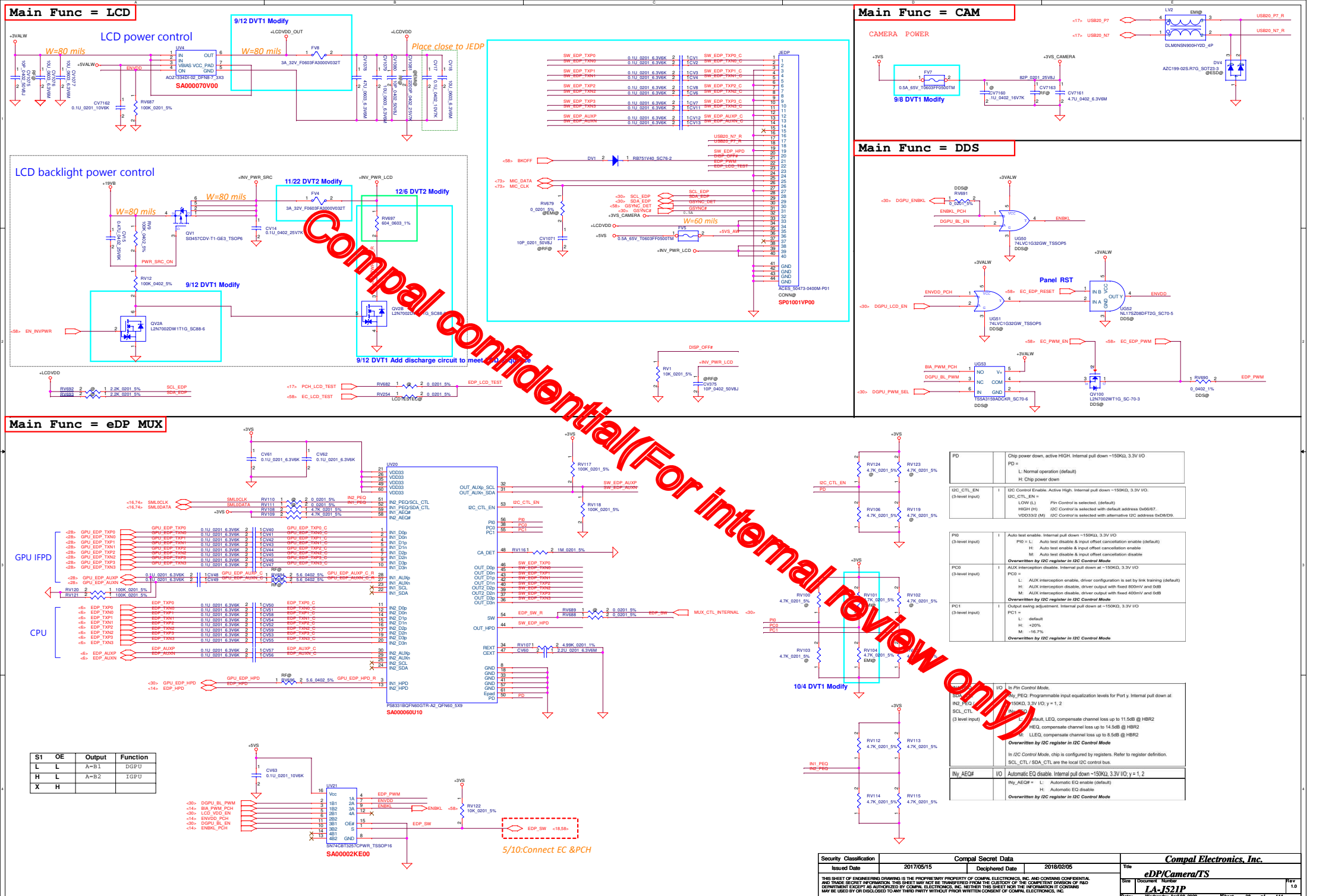
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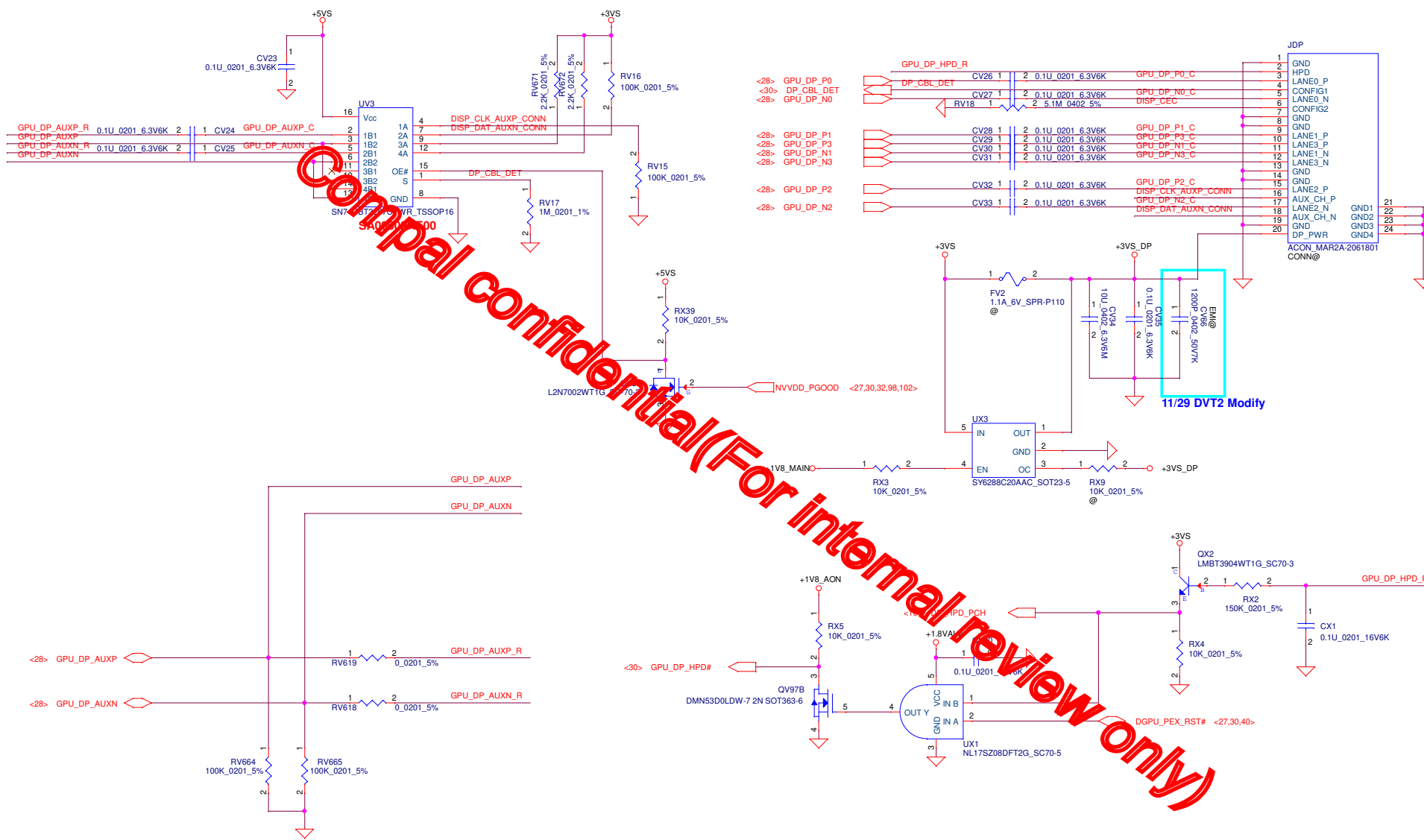
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				Size	Document Number
				LA-J521P	Rev 1.0
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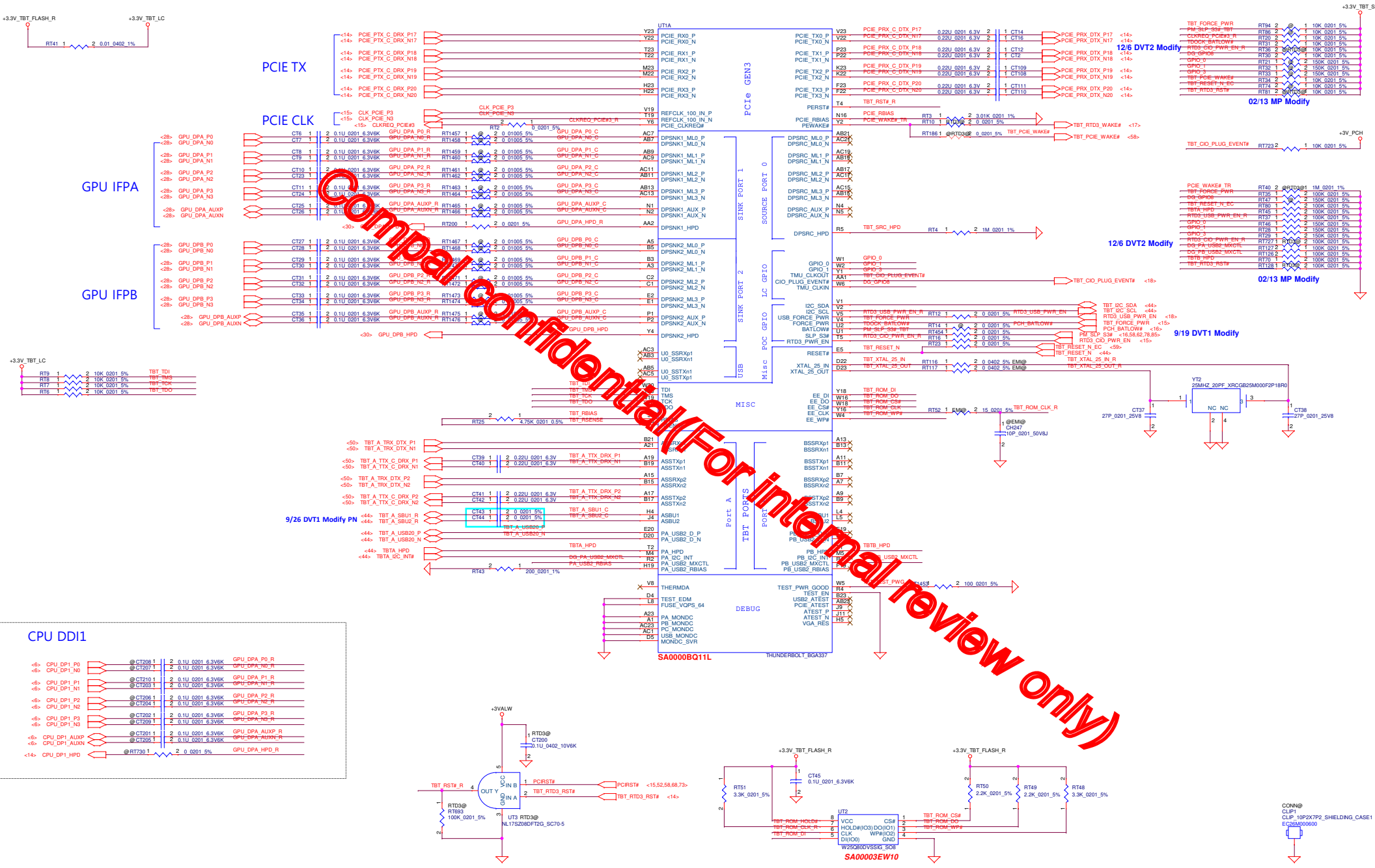


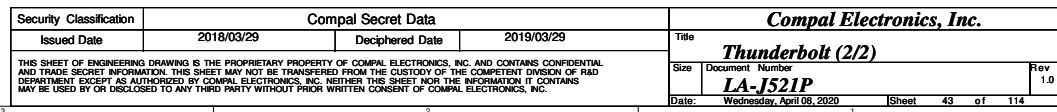
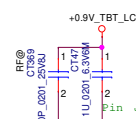


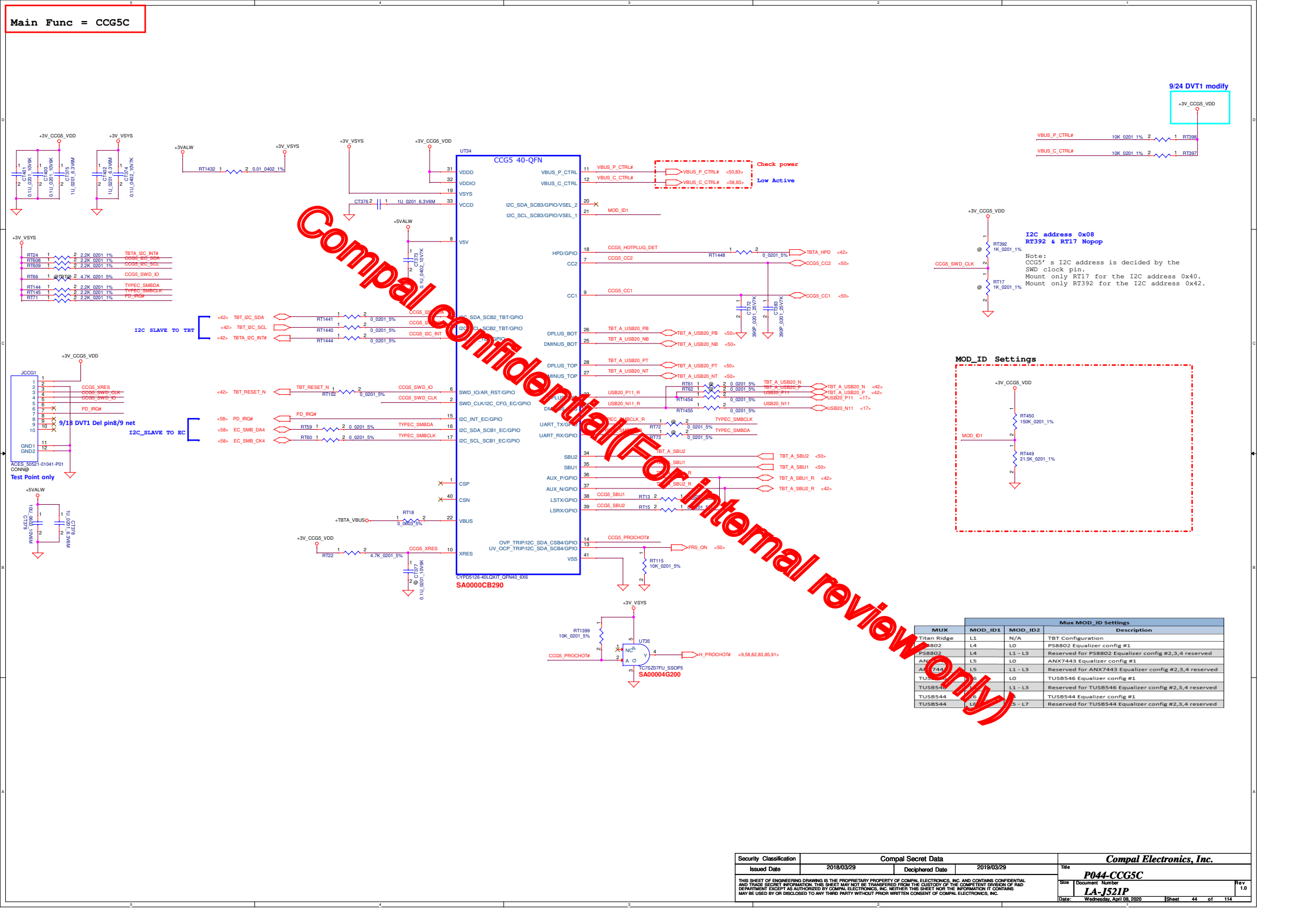
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Issued Date		2017/05/15		Deciphered Date		2018/02/05		Title			
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								Size Document Number			
								LA-J521P			
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				LA-J521P	
				Date: Wednesday, April 08, 2020	Rev 1.0
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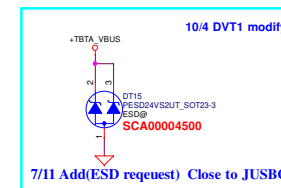
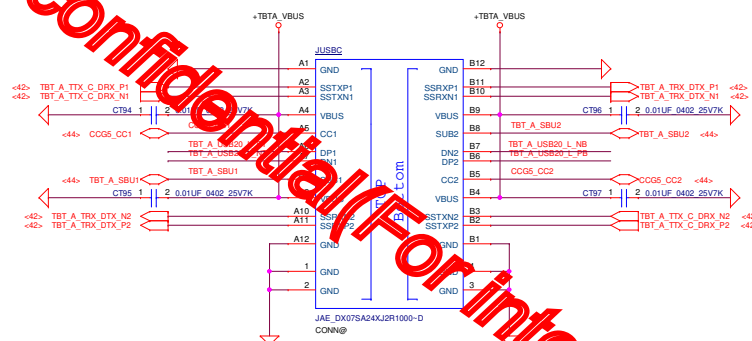
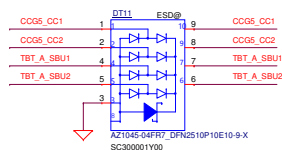
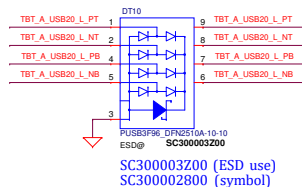
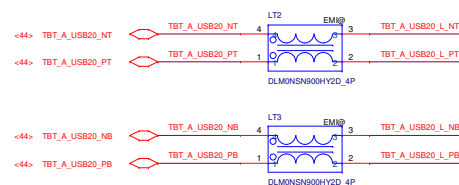
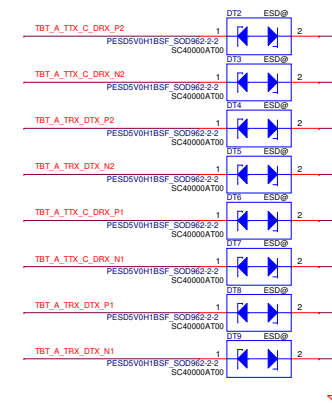
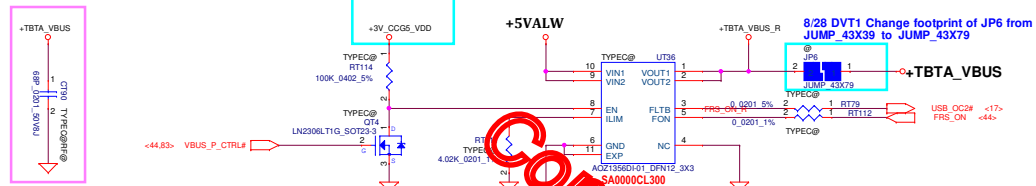
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CCG5 Power path Port1

Type-C 5V Provide Path Control
Support PD3.0
5V@3A

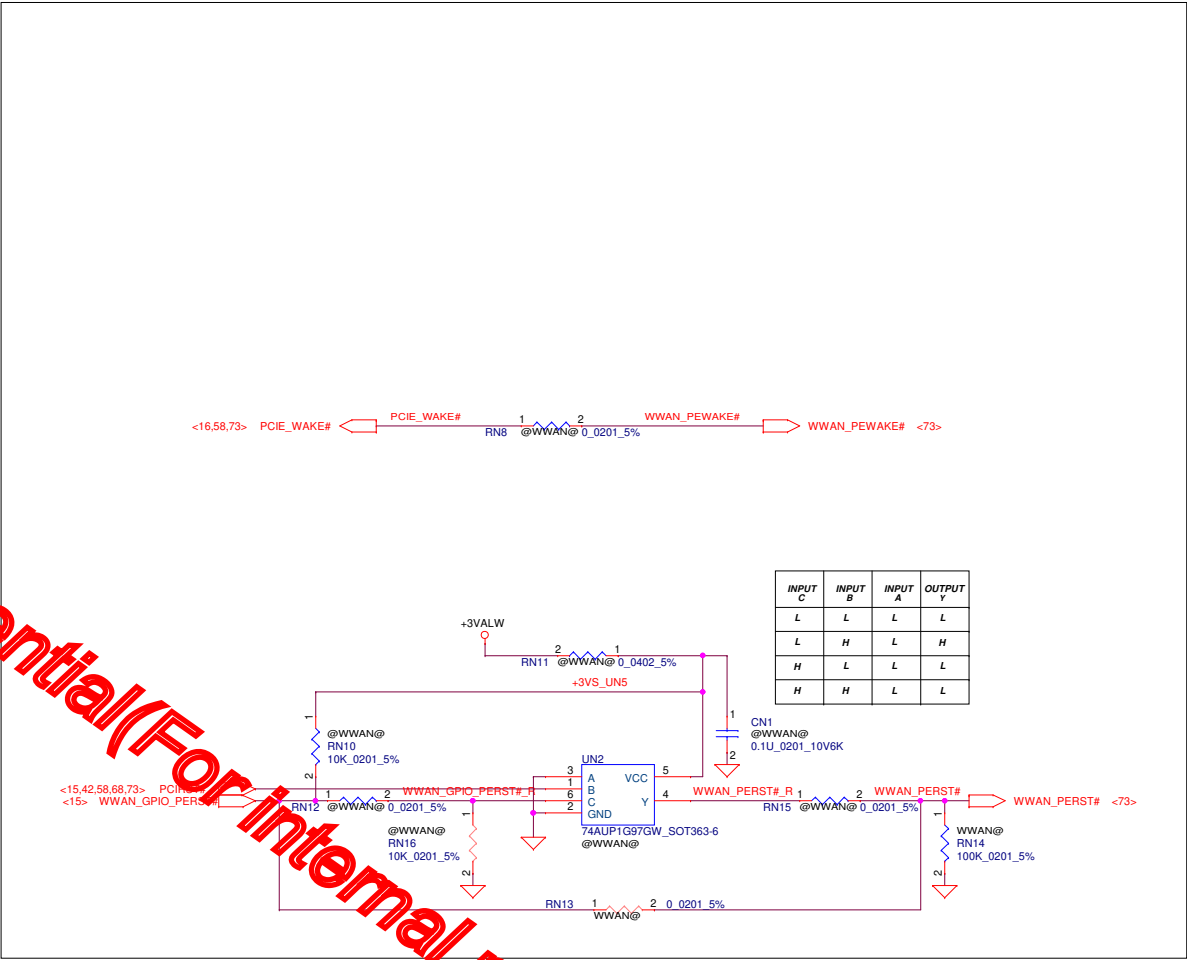


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				LA-J521P	
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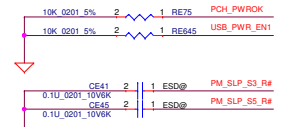
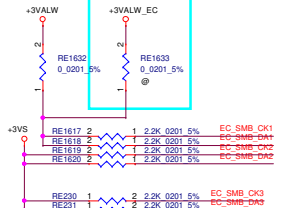
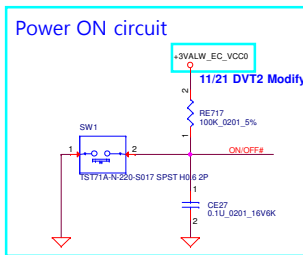
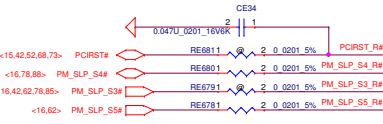
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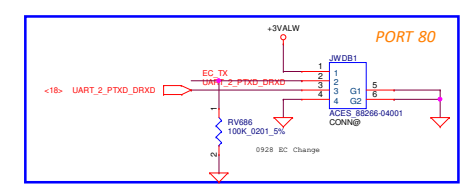
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				LA-J521P	
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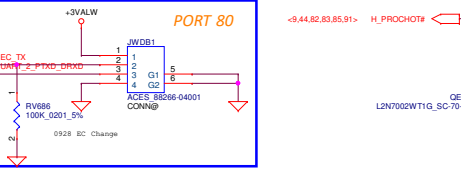
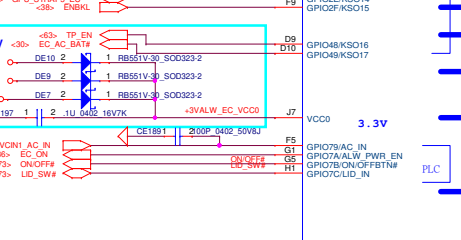
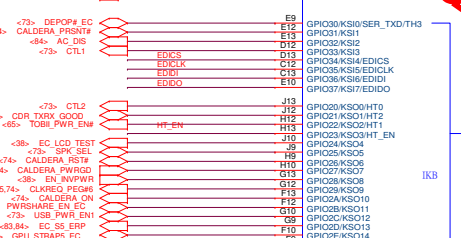
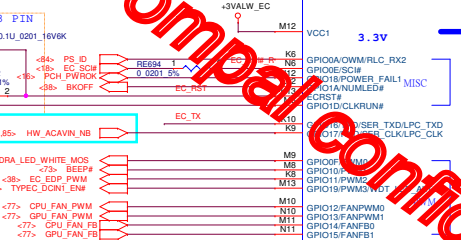
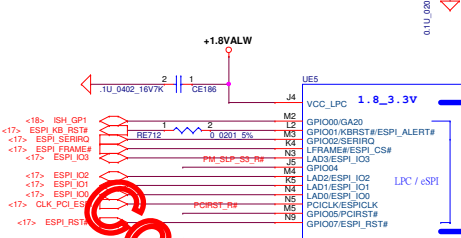
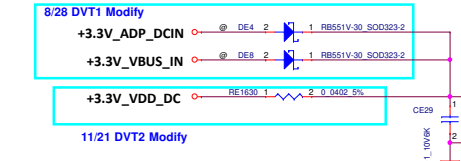
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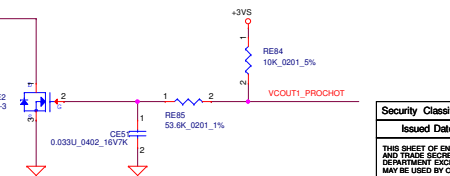
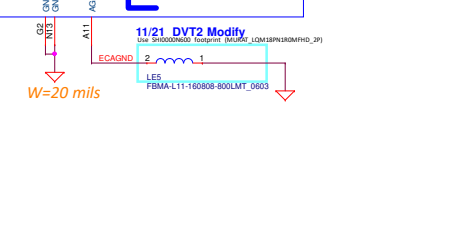
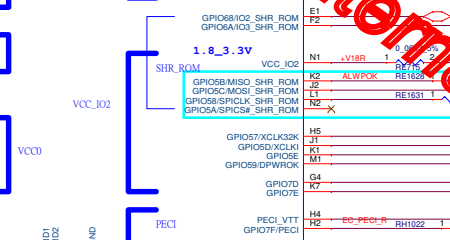
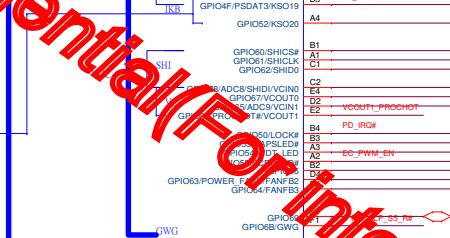
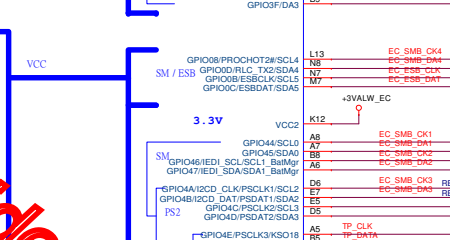
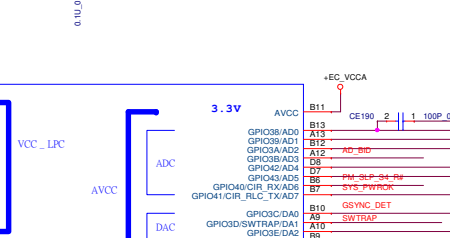
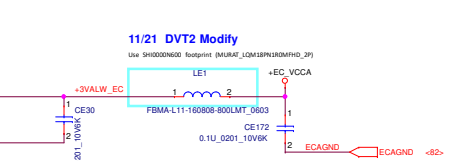
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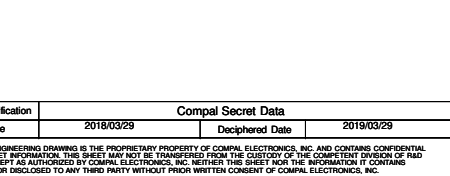
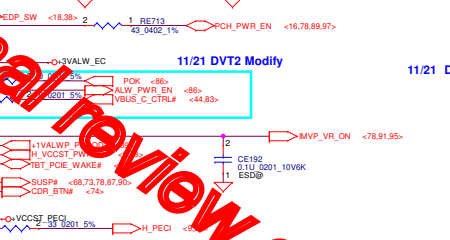
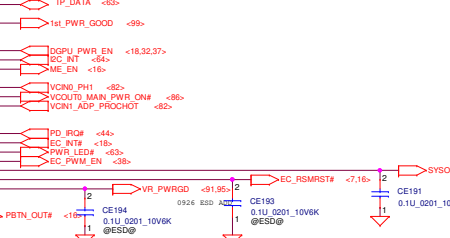
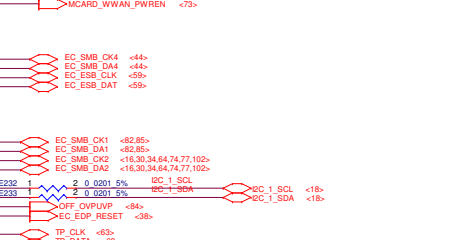
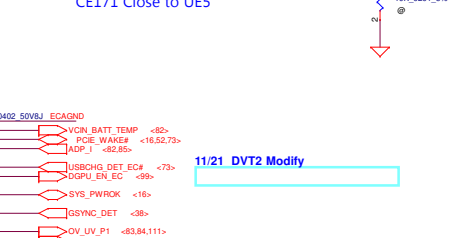
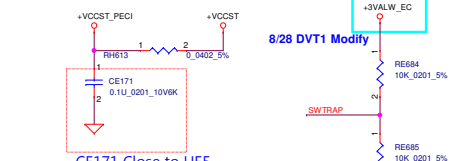
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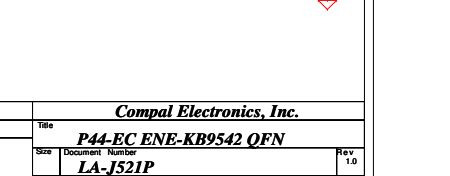
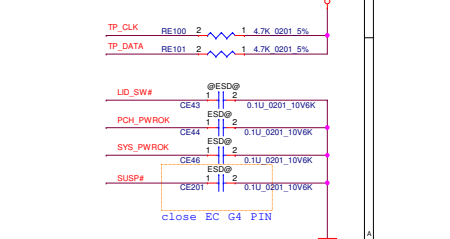
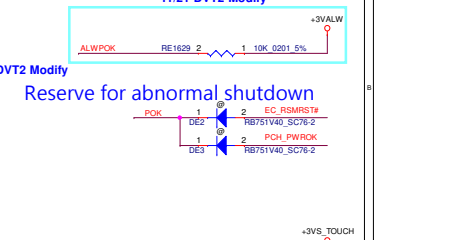
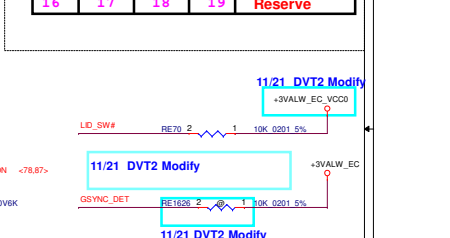
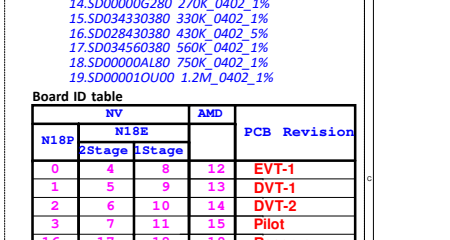
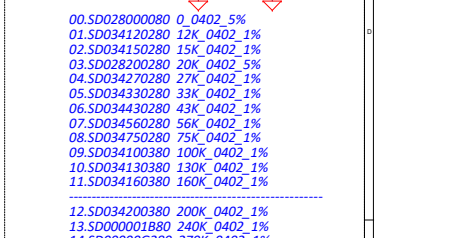
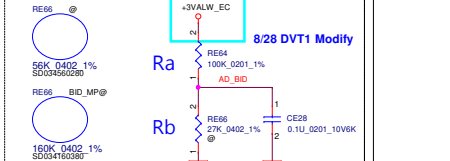
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0921 update



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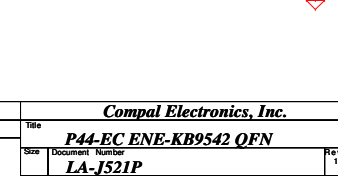
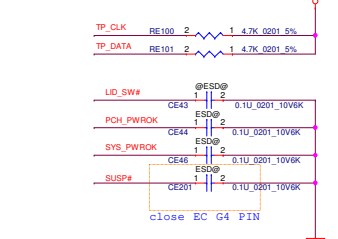
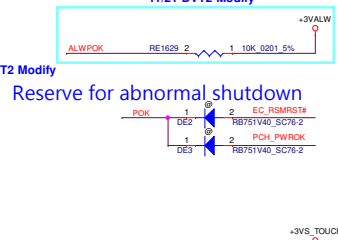
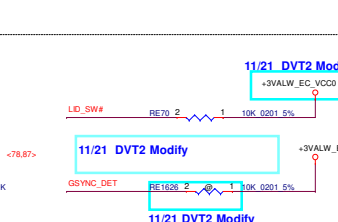


0921 update

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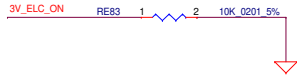
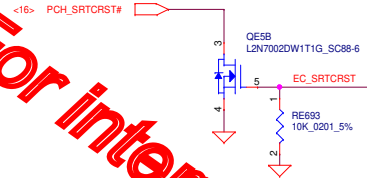
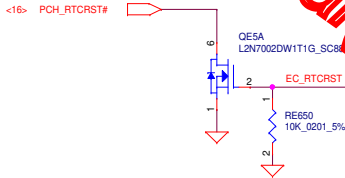
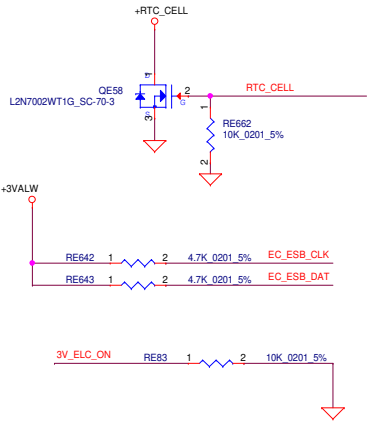
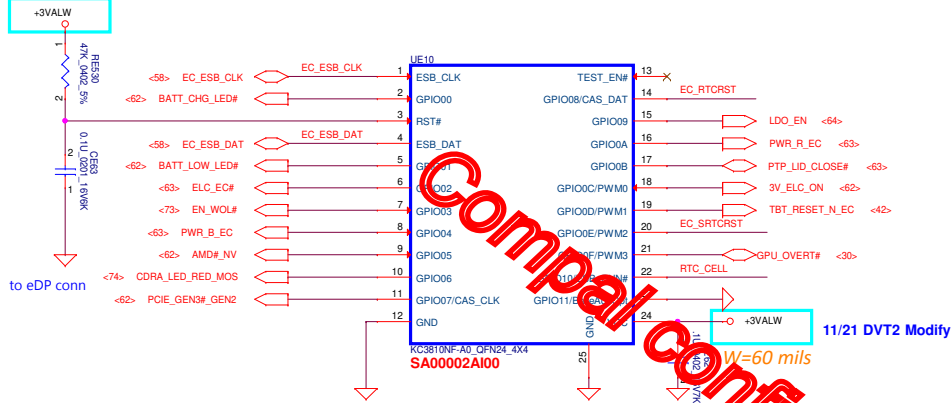


0921 update

Main Func = EC ENE-KC3810

Main Func = S5 Lid

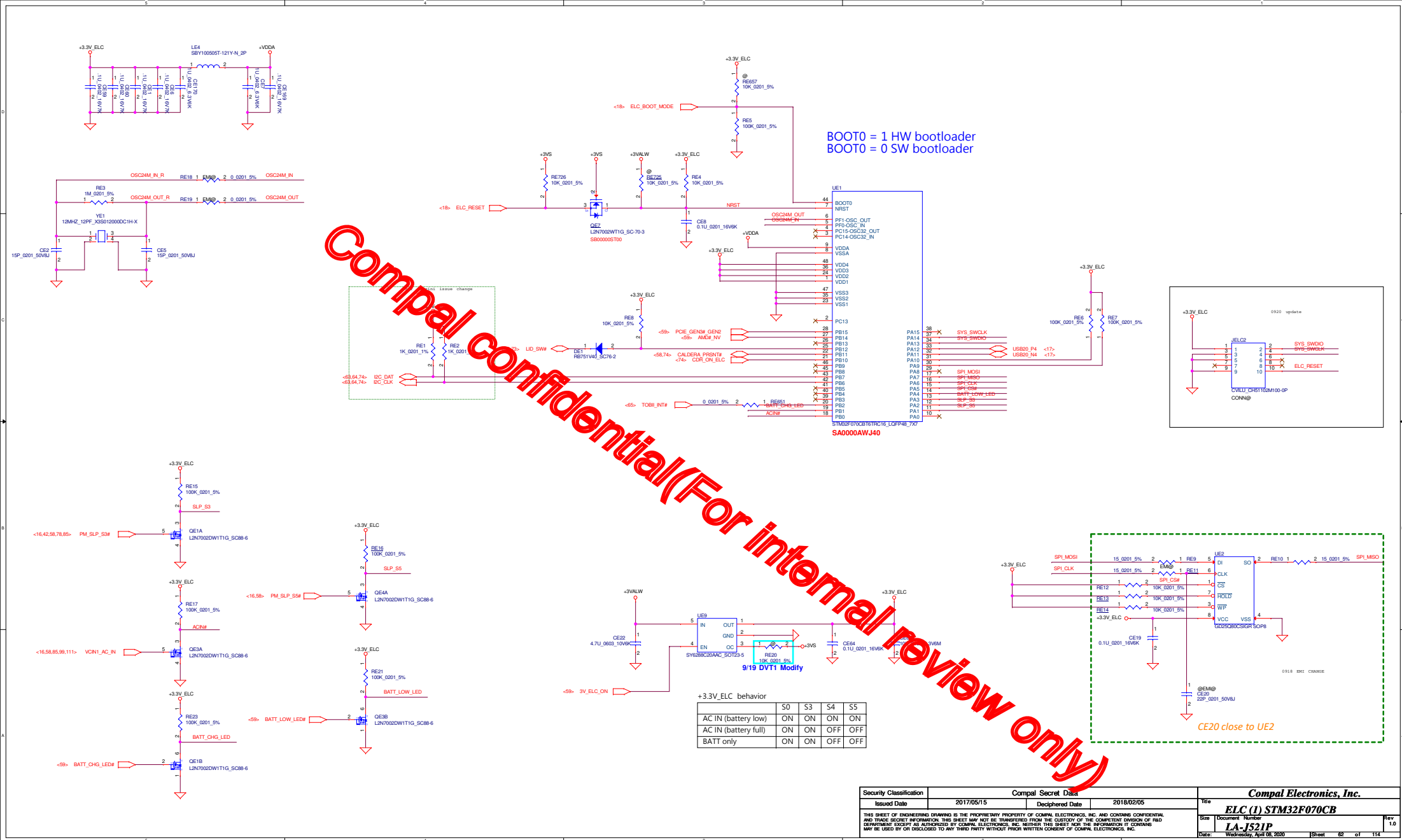
11/21 DVT2 Modify



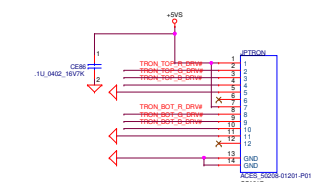
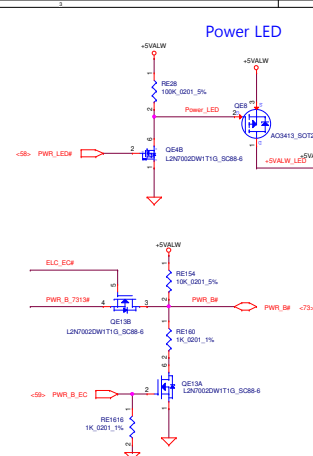
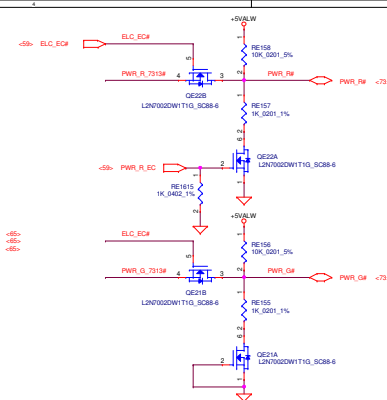
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/03/29	Deciphered Date	2018/03/29	Title	EC ENE-KB9022/S5 LID	
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					LA-J521P	1.0
				Date:	Wednesday, April 06, 2020	Sheet 59 of 114

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				LA-J521P	
				Date: Wednesday, April 08, 2020	Rev 1.0
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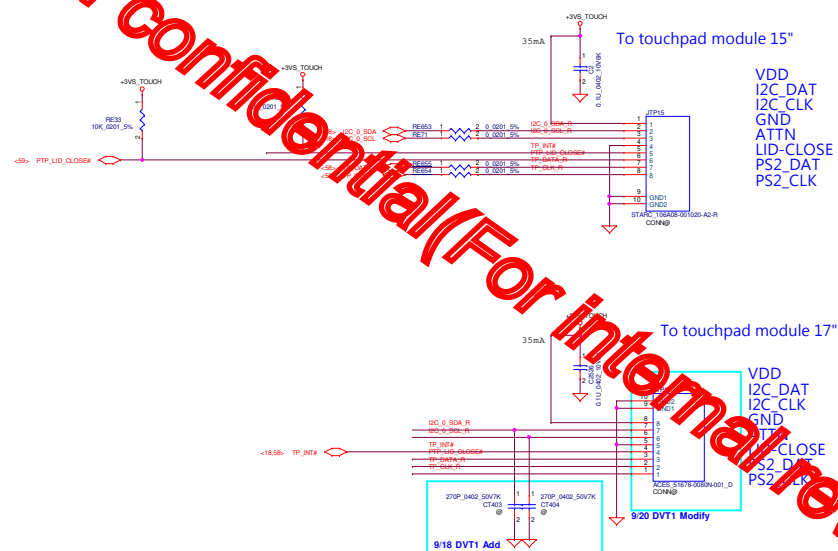
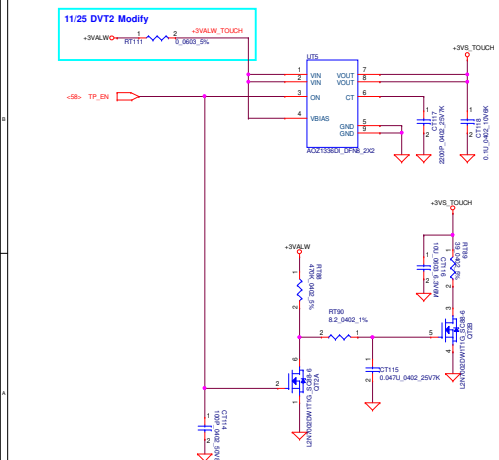
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AD0 0
AD1 0
AD2 1
AD3 0
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9/18 DVT1 Add

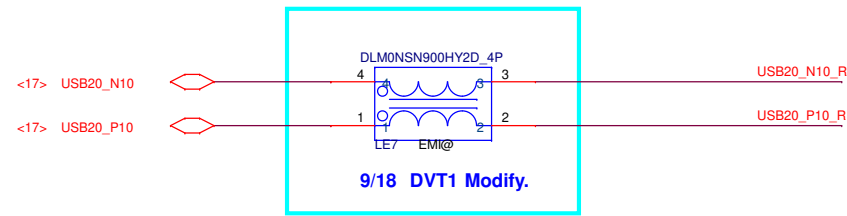
9/20 DVT1 Modify

Rev	Classification	Issued Date	2017/05/15	Compal Se	Deci
1	Engineering Drawing	2017/05/15			

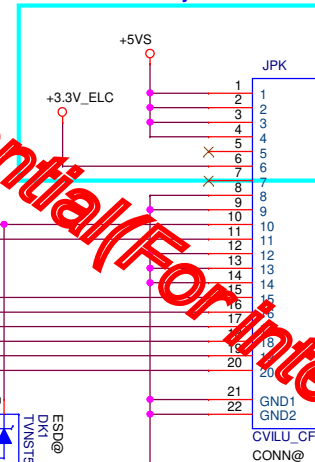


8/28 DVT1 Del Tron-Primax solution

Classification Exempt Date 2017/05/15 Declassified Date 2018/02/05	Compul Secret Data 2018/02/05	Title Compul Electronics, Inc. ELC (2) TP/PW/LOGO/TRON	Date 2017/05/15 Document LA-1521	Sheet 03 of 14
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11/21 DVT2 Modify.

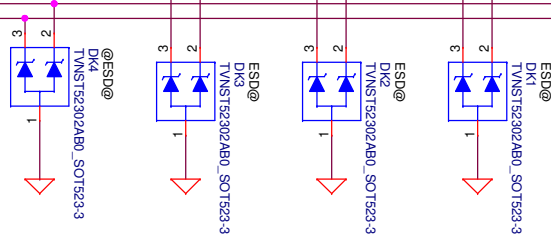


Per Key pin define

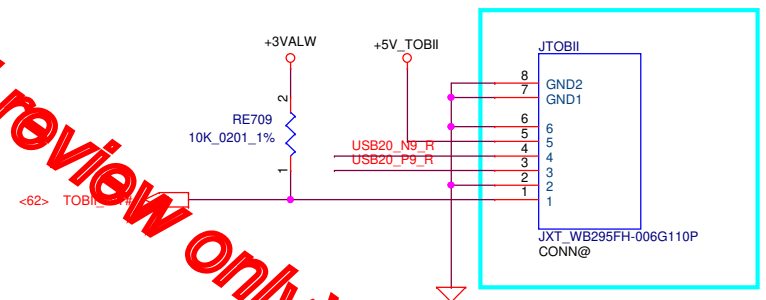
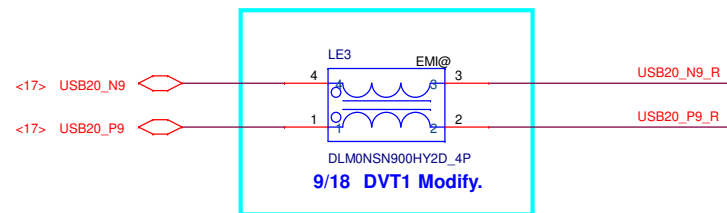
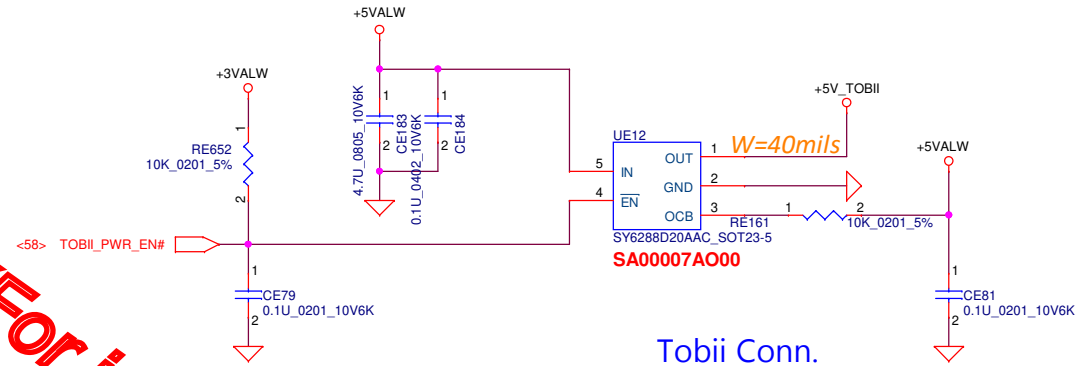
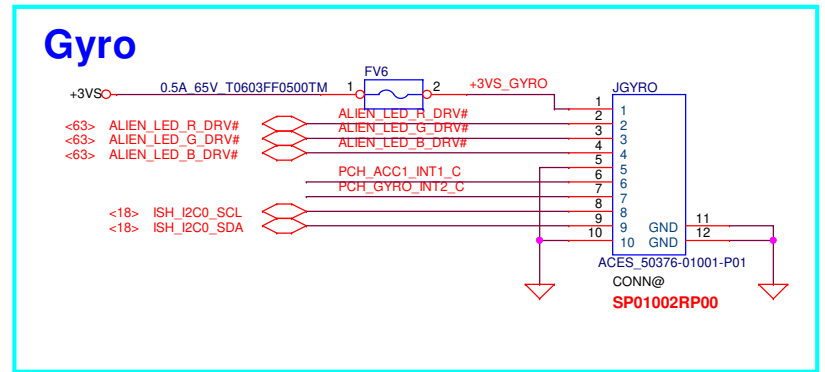
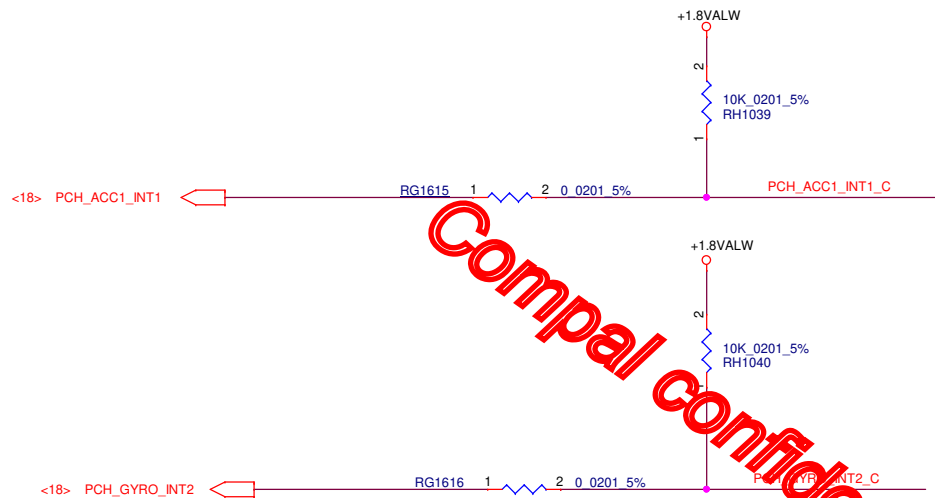
Pin1~4 VBUS
Pin5 NC
Pin6 +3.3V_ELC
Pin7 NC
Pin8~9 GND
Pin10 D-
Pin11 D+
Pin12~14 GND
Pin15 I2C_INT
Pin16 I2C_CLK(EC)
Pin17 I2C_DAT(EC)
Pin18 LDO_EN
Pin19 I2C_CLK(ELC)
Pin20 I2C_DAT(ELC)

<58> I2C_INT
<16,30,34,58,74,77,102> EC_SMB_CK2
<16,30,34,58,74,77,102> EC_SMB_DA2
<59> LDO_EN
<62,63,74> I2C_CLK
<62,63,74> I2C_DAT

+3VS
RE656
10K_0402_5%



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Size		Document Number			Rev
		LA-J521P			1.0
Date:		Wednesday, April 08, 2020		Sheet	64 of 114



8/28 DVT1 Modify JTOBII footprint to JXT_WB295FH-006G110P_6P-T

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				Size	Document Number
				LA-J521P	
Date: Wednesday, April 08, 2020		Sheet 65 of 114		Rev 1.0	

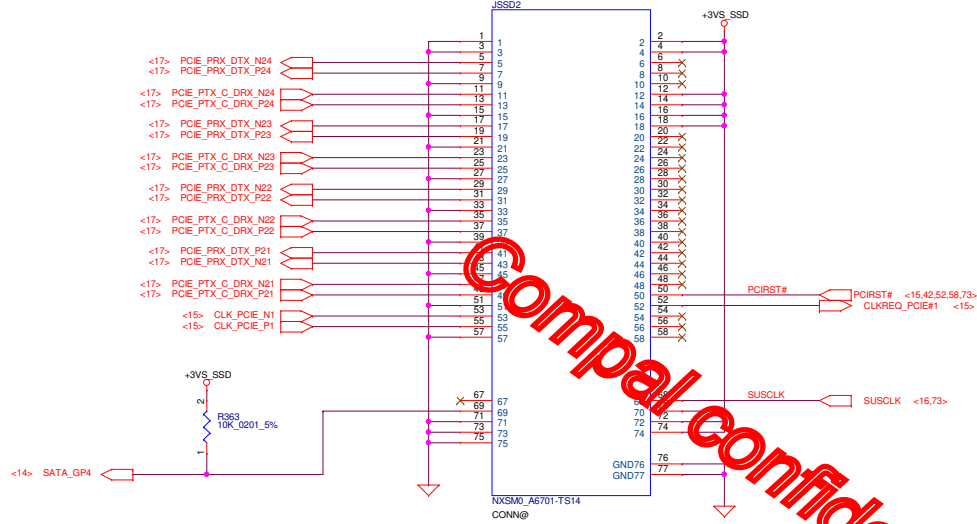
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				LA-J521P	
				Date: Wednesday, April 08, 2020	Rev 1.0
				Sheet 66 of 114	

Compal confidential (For internal review only)

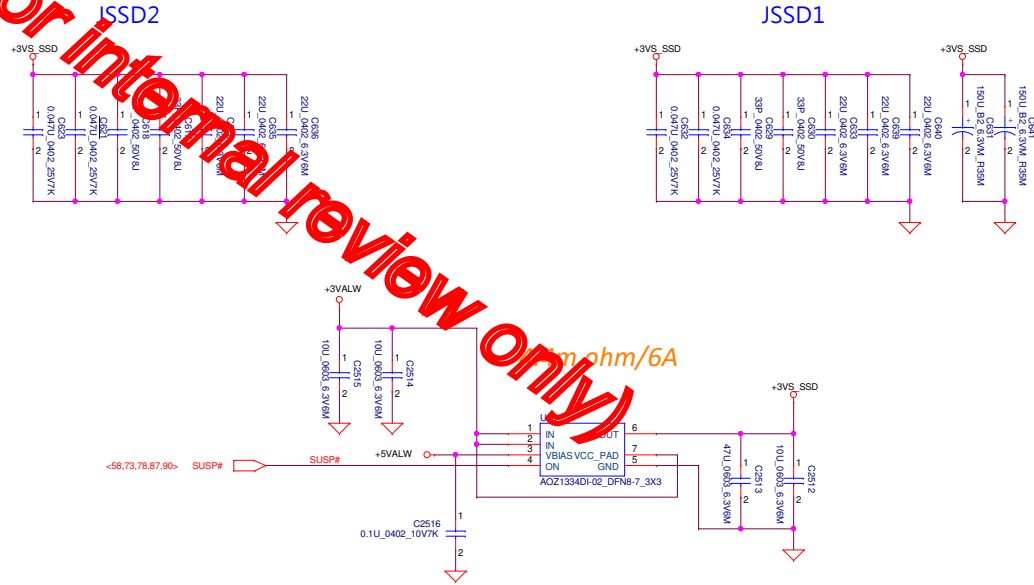
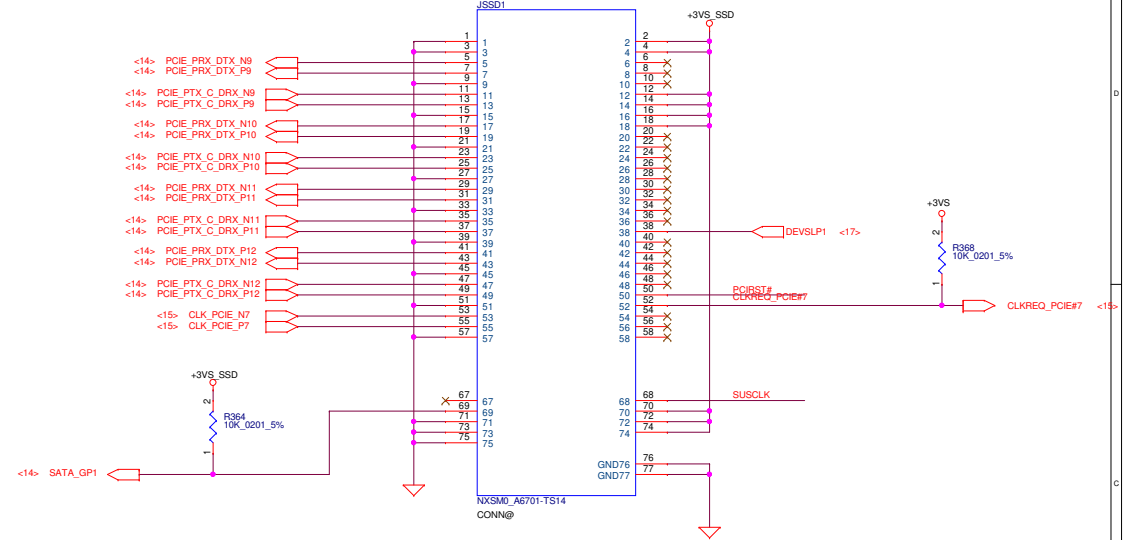
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				Sheet 67 of 114	

PCIe SSD#2 , 2280



PEDET	Module Type
0	SATA
1	PCIe

PCIe / SATA SSD SSD#1 , 2280



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				LA-J521P	
				Date: Wednesday, April 08, 2020	Rev 1.0
				Sheet 70 of 114	

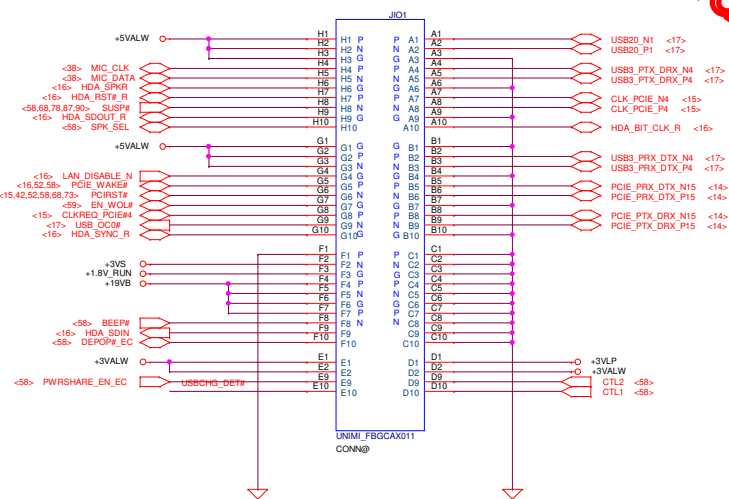
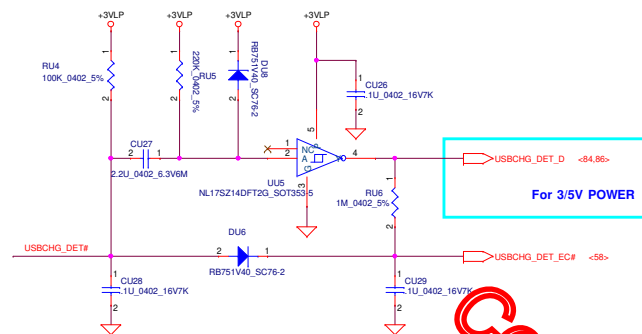
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				LA-J521P	
				Date: Wednesday, April 08, 2020	Rev 1.0
				Sheet 71 of 114	

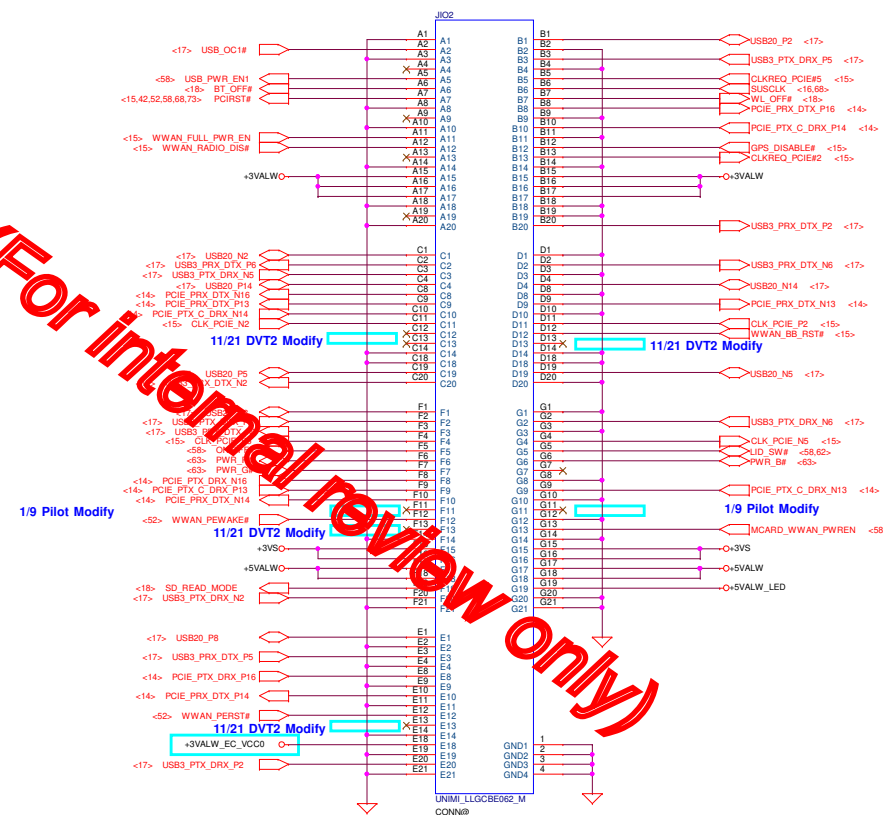
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				LA-J521P	
				Date: Wednesday, April 08, 2020	Rev 1.0
				Sheet 72 of 114	

USB charge for DC S5

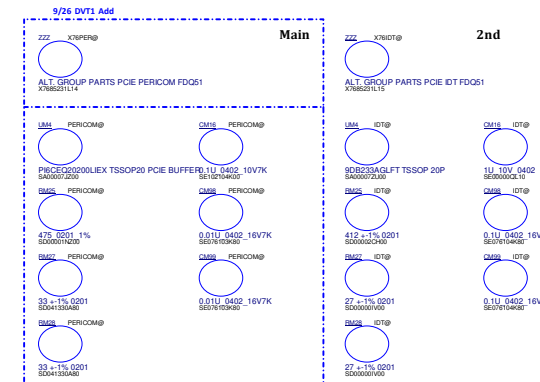


For Audio DB conn

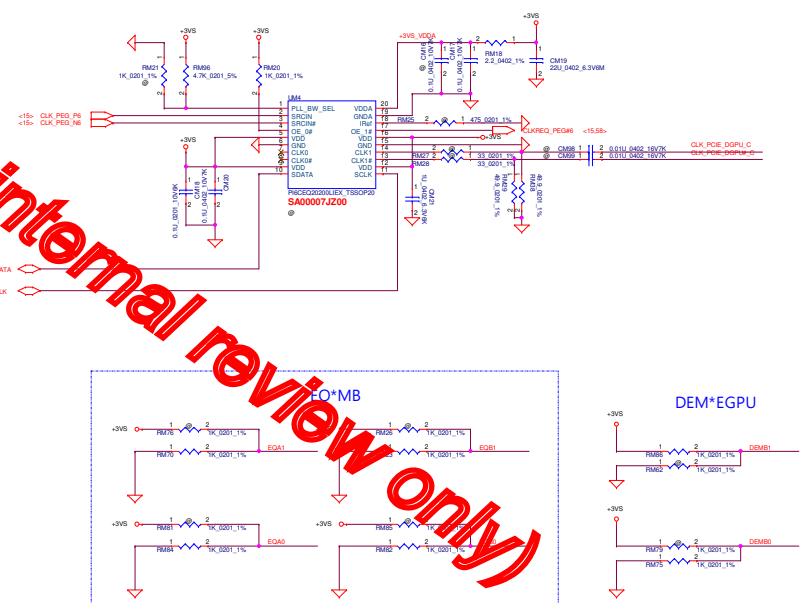


For USB DB conn

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PCIE Clock Buffer	RM25	RM27 / RM28	CM16	CM98 / CM99
Pericom (S40007J200) X768231.14	SD00001N200 (475 ±1% Q201)	SD041330A80 (33 ±1% Q201)	SE102104K00 (0.1U ±10% Q402)	SE076103K80 (0.01U 16V K X7R Q402)
IDT (S40007ZU00) X768231.15	SD00000C200 (412 ±1% Q201)	SD000001V00 (27 ±1% Q201)	SE00000QL10 (1U ±10% Q402)	SE076104K80 (0.1U 16V K X7R Q402)



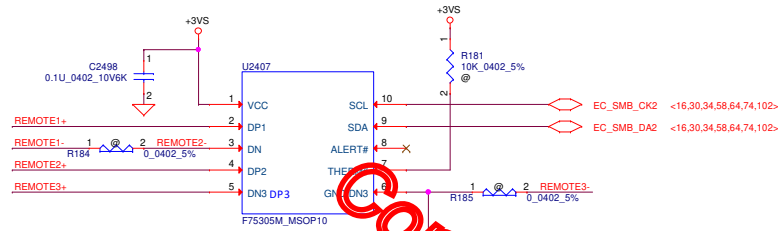
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					LA-J521P
				Date:	Wednesday, April 08, 2020
				Sheet	76 of 114
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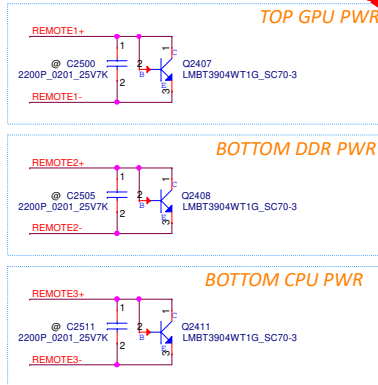
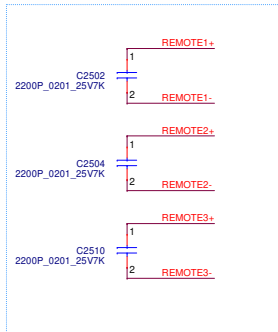
Fintek thermal sensor---> CPU core, DIMM



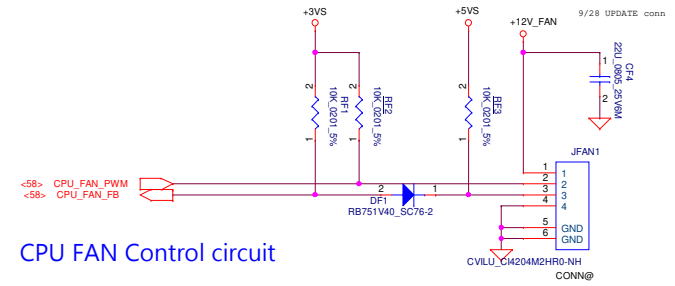
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2nd source
SA000029210-->EMC1403-2-AIZL-TR

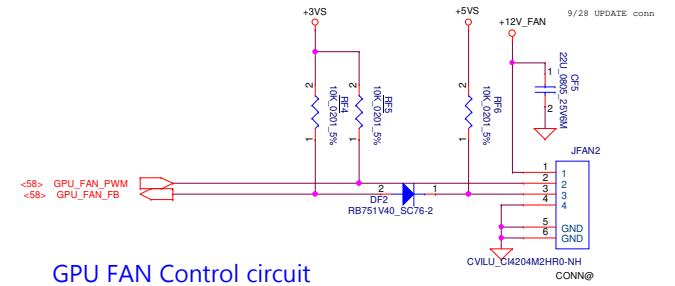
Close U2407



REMOTE1+ (-) :
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Trace length :

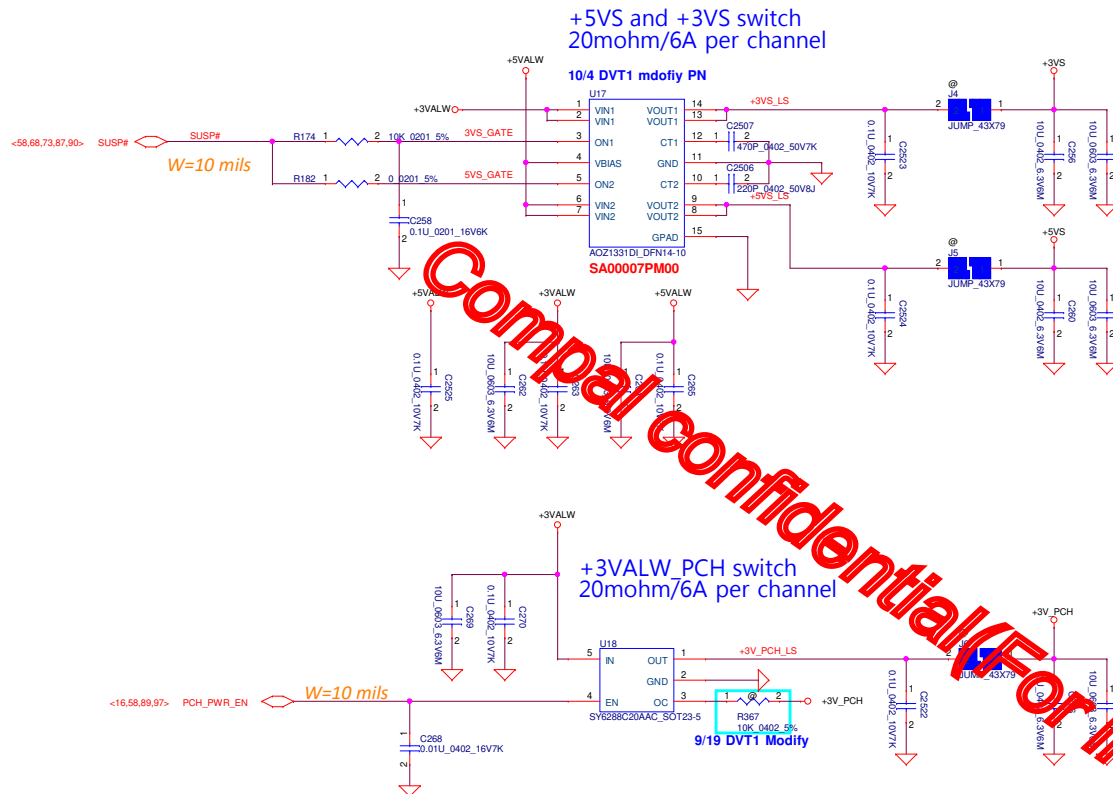


CPU FAN Control circuit



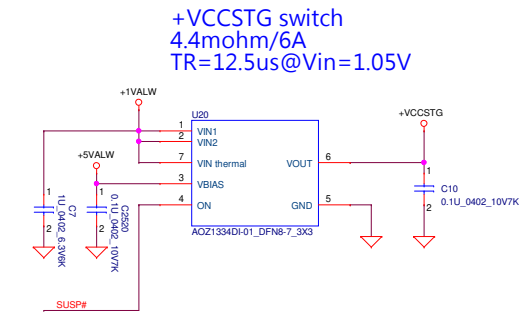
GPU FAN Control circuit

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Size	Document Number	Rev	1.0	
Date:	Wednesday, April 08, 2020	Sheet	77	of 114

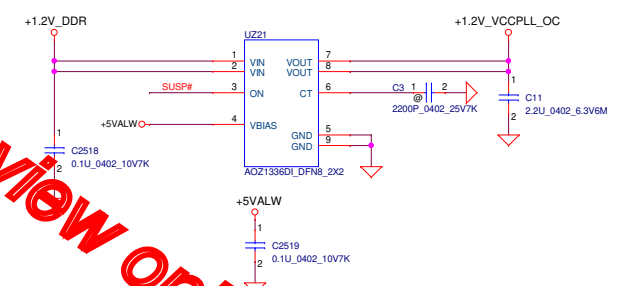


Main source
2nd source
3rd source

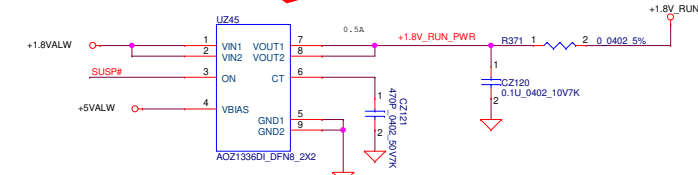
ACS SA00008A800 (SI C ACZ1334DI-01 DFN8-7_3X3)
APEC SA00006V300 (SI C APE8939GNB DFN8-7_3X3)
E MC SA00008R600 (SI C E M5201V DFN8-7_3X3)



+1.2V_VCCPLL_OC switch
4.4mohm/6A
TR=12.5us@Vin=1.05V



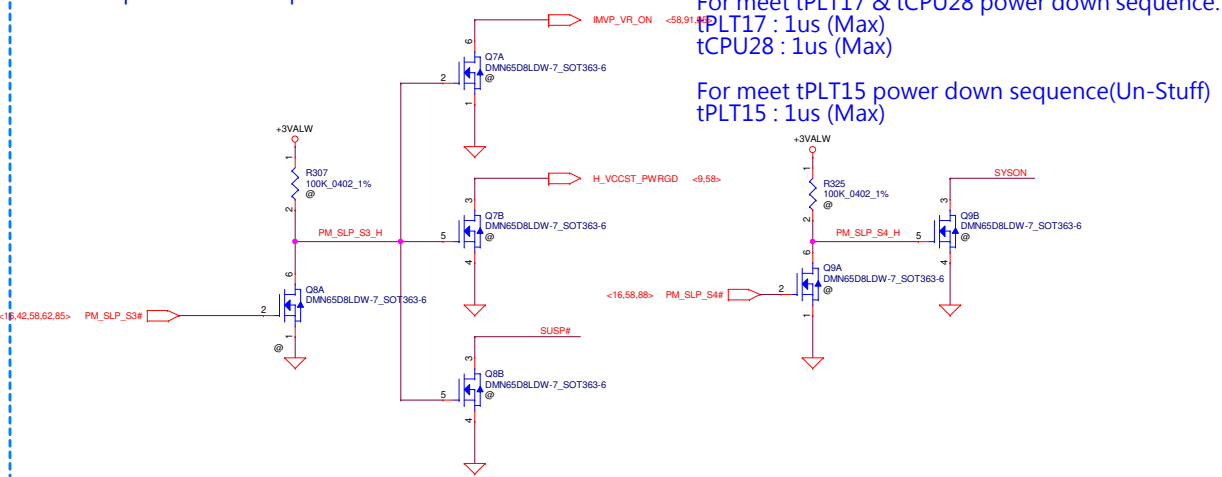
+1.8V_RUN Source



add for power down sequence

For meet tPLT17 & tCPU28 power down sequence
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)

For meet tPLT15 power down sequence(Un-Stuff)
tPLT15 : 1us (Max)

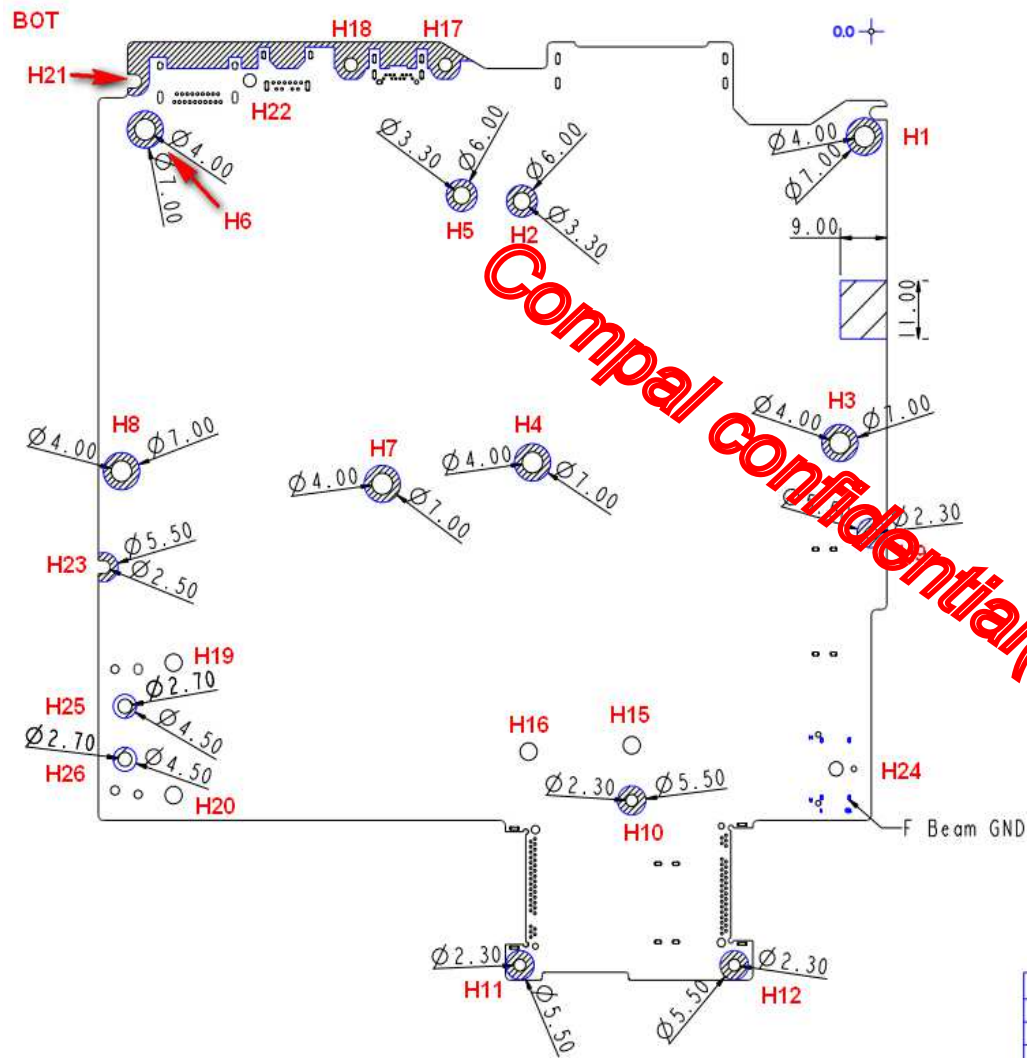


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Sheet		78		of 114	

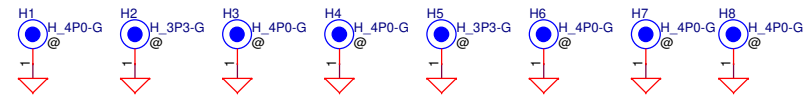
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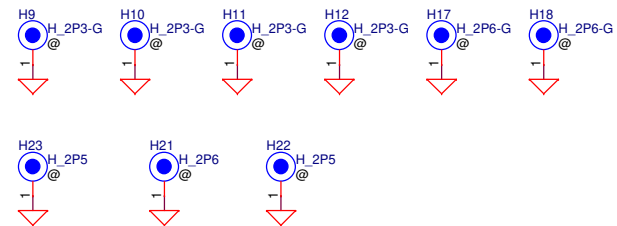
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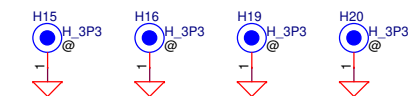
CPU & GPU



PTH



Stand-off

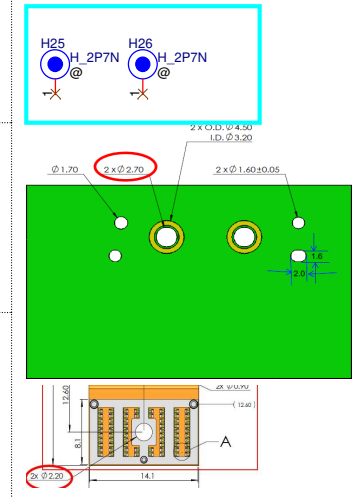


Fiducial Mark



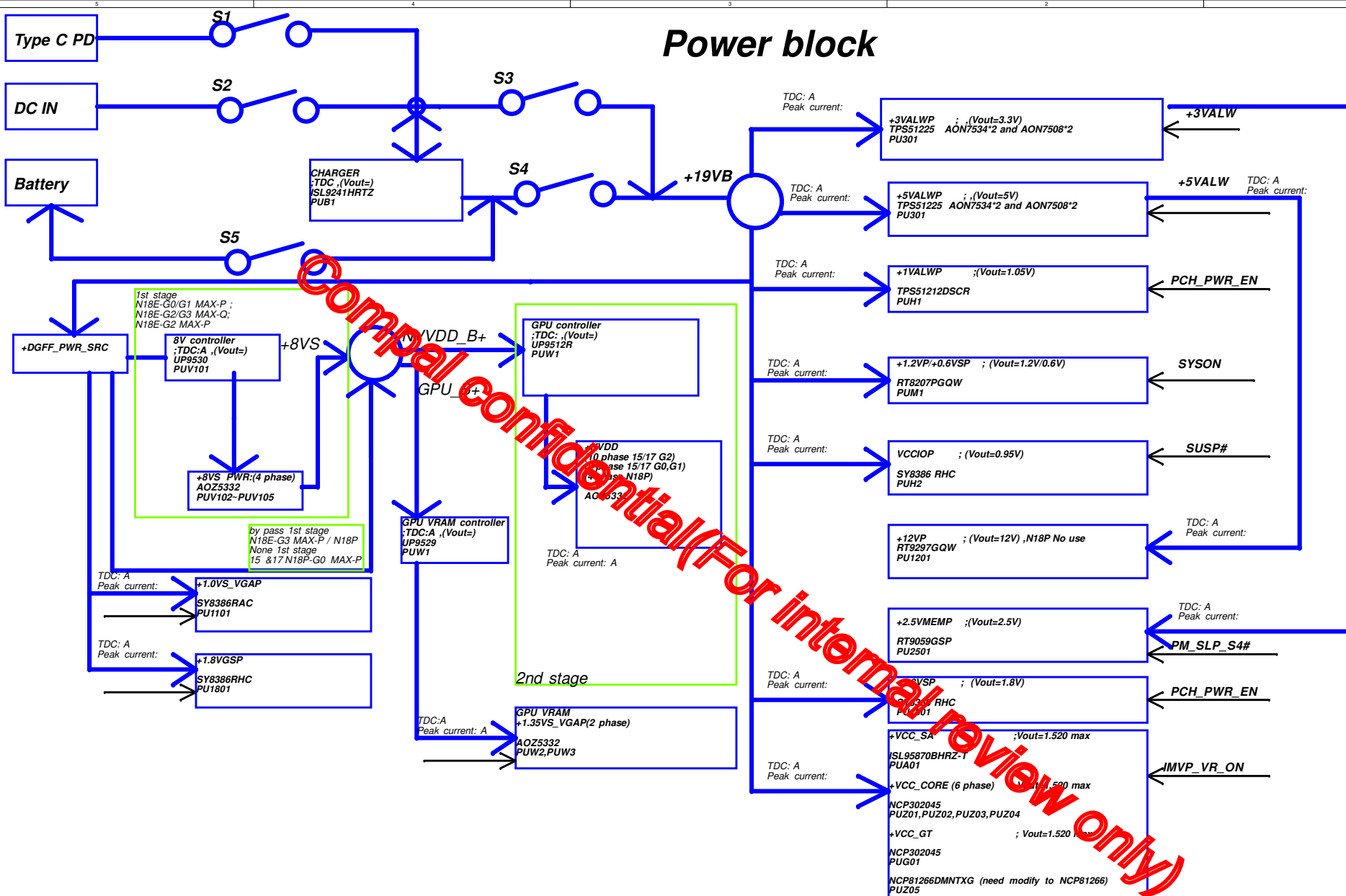
PC-Beam (Stand-off)

11/21 DVT2 Add



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				Size	Document Number
				LA-J521P	
				Date:	Wednesday, April 08, 2020
				Sheet	80 of 114
				Rev	1.0

Power block



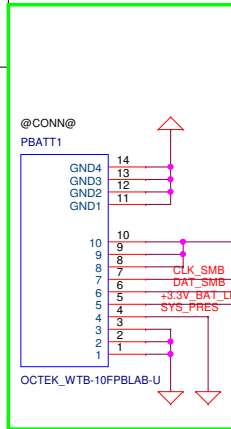
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title		
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				Size	Document Number	Rev
					LA-J521P	0.3
				Date:	Wednesday, April 08, 2020	Sheet 81 of 114

Battery 86W
86W/9V=9.56A

Battery connector:

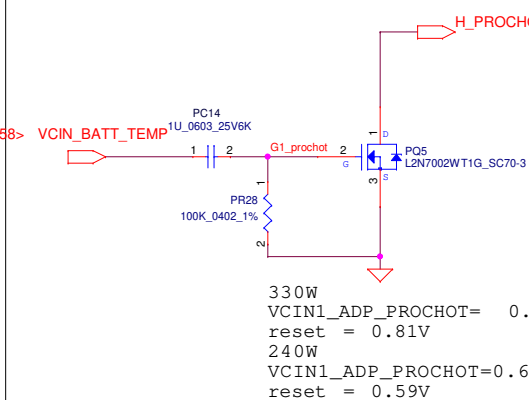
- 1.GND
- 2.GND
- 3.GND
- 4.SYS_PRES
- 5.BATT_PRS
- 6.DAT_SMB
- 7.CLK_SMB
- 8.BATT++
- 9.BATT++
- 10.BATT++

confirm PJPBATT pin

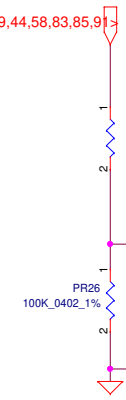


battery unplug proshot

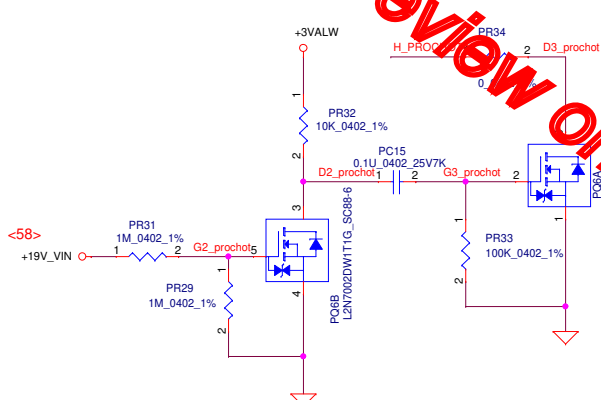
For PROCHOT



<58,85> ADP_I

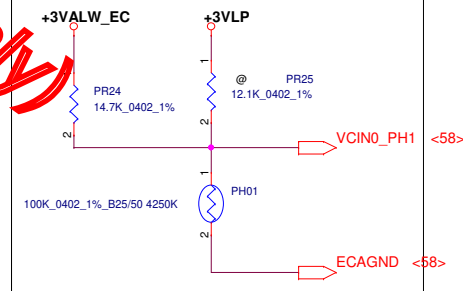


adapter unplug proshot



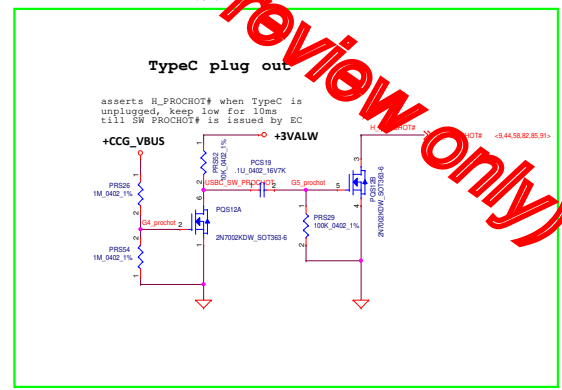
CPU thermal protection

VCIN0_PH
Trig = 1V
93 +/- 3 degree C
Recover = 2.28V
50 +/- 3 degree C



Security Classification			
Compal Secret Data			
Issued Date	2017/05/15	Deciphered Date	2017/01/06
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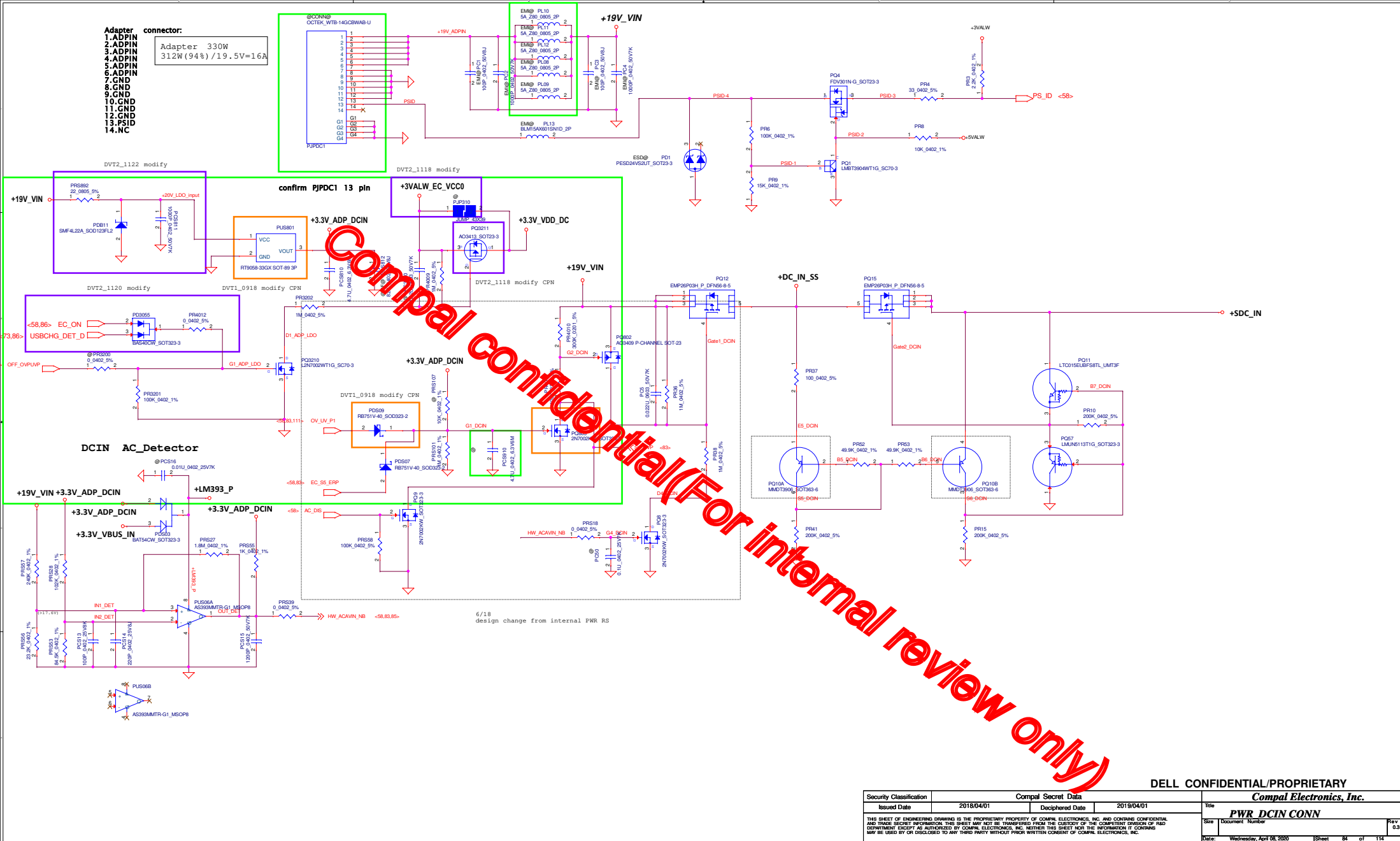
Compal Electronics, Inc.			
Title			
PWR-DCIN / BATT CONN / OTP			
Size	Document Number	Rev	
	LA-J521P	0.3	
Date:	Wednesday, April 08, 2020	Sheet	82 of 114



Security Classification	Compal Secret Data		Title	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	File
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Date: Wednesday, April 19, 2025			Sheet	85 of 114

Adapter
1.ADPIN
2.ADPIN
3.ADPIN
4.ADPIN
5.ADPIN
6.ADPIN
7.GND
8.GND
9.GND
10.GND
11.GND
12.GND
13.PSID
14.NC

connector:
Adapter 330W
312W (94%) / 19.5V=16A



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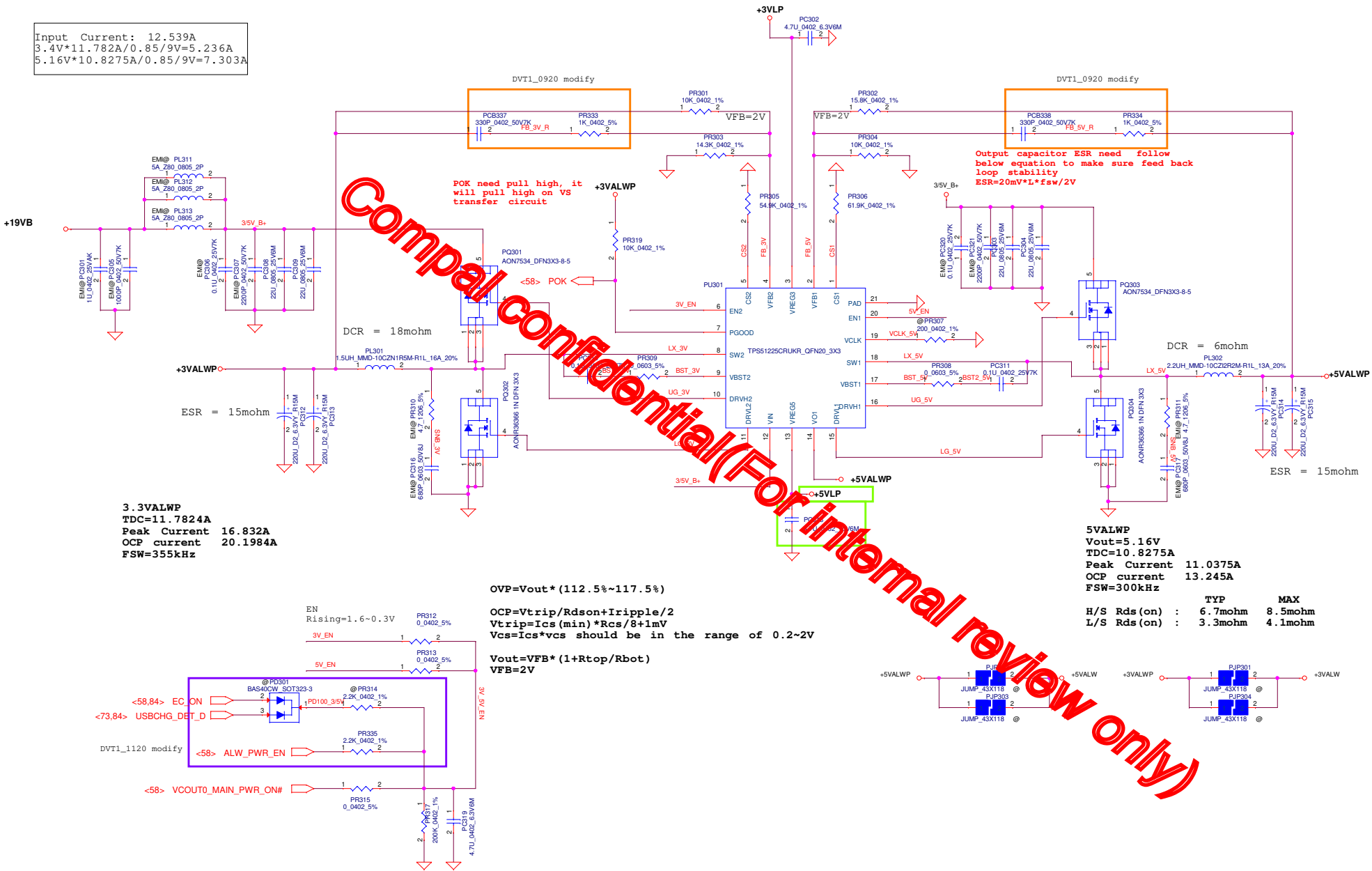
Battery information:
3S1P (3cells/3S2P(6cell)
12.6V/ 86Wh (nominal) ; 12.6V/56Wh
Charge Voltage: 13.2V (CC-CV Mode)
Rated Charge Current: mAh (normal)
Fast charging : mA(1C/50%)
Update by 2019/5/28

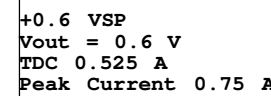
Notice:

BAT_DET#
H: >4.6V (Battery remove).
L: <4.1V (Battery plug in).
(2018/10/19)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/05/15	Dispersed Date	2018/12/01	Doc No.	PWR_Charger
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Date	Wednesday, April 26, 2020	Sheet	85	of	112

Input Current: 12.539A
 $3.4V \times 11.782A / 0.85 / 9V = 5.236A$
 $5.16V \times 10.8275A / 0.85 / 9V = 7.303A$

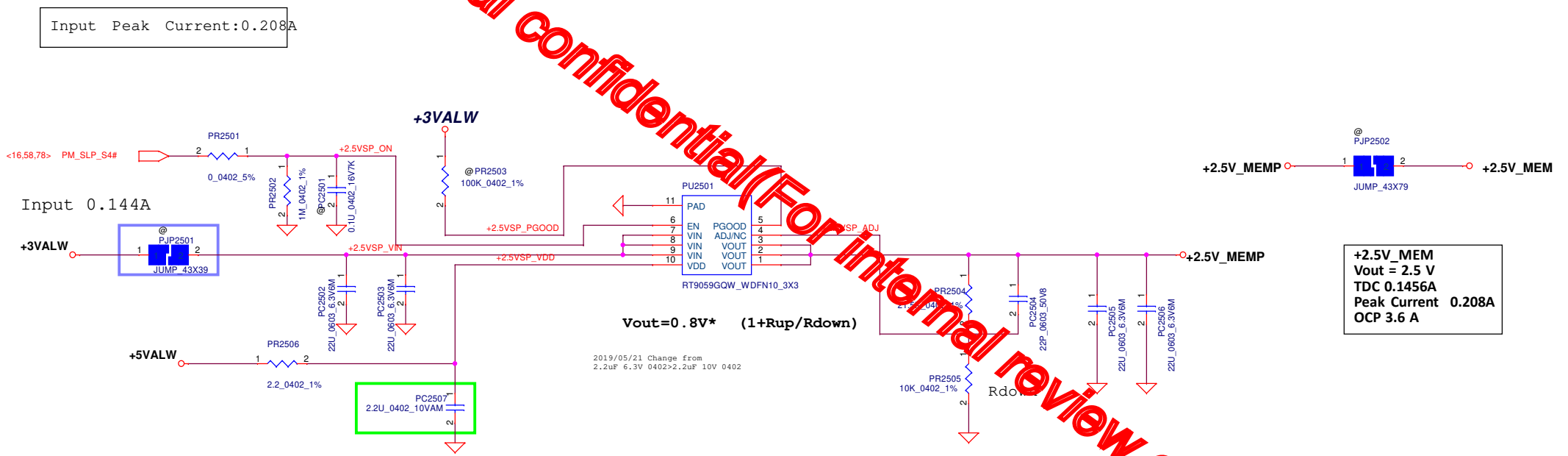


$$1.2V \cdot 6.68A / 0.85 / 9V = 1.047A$$


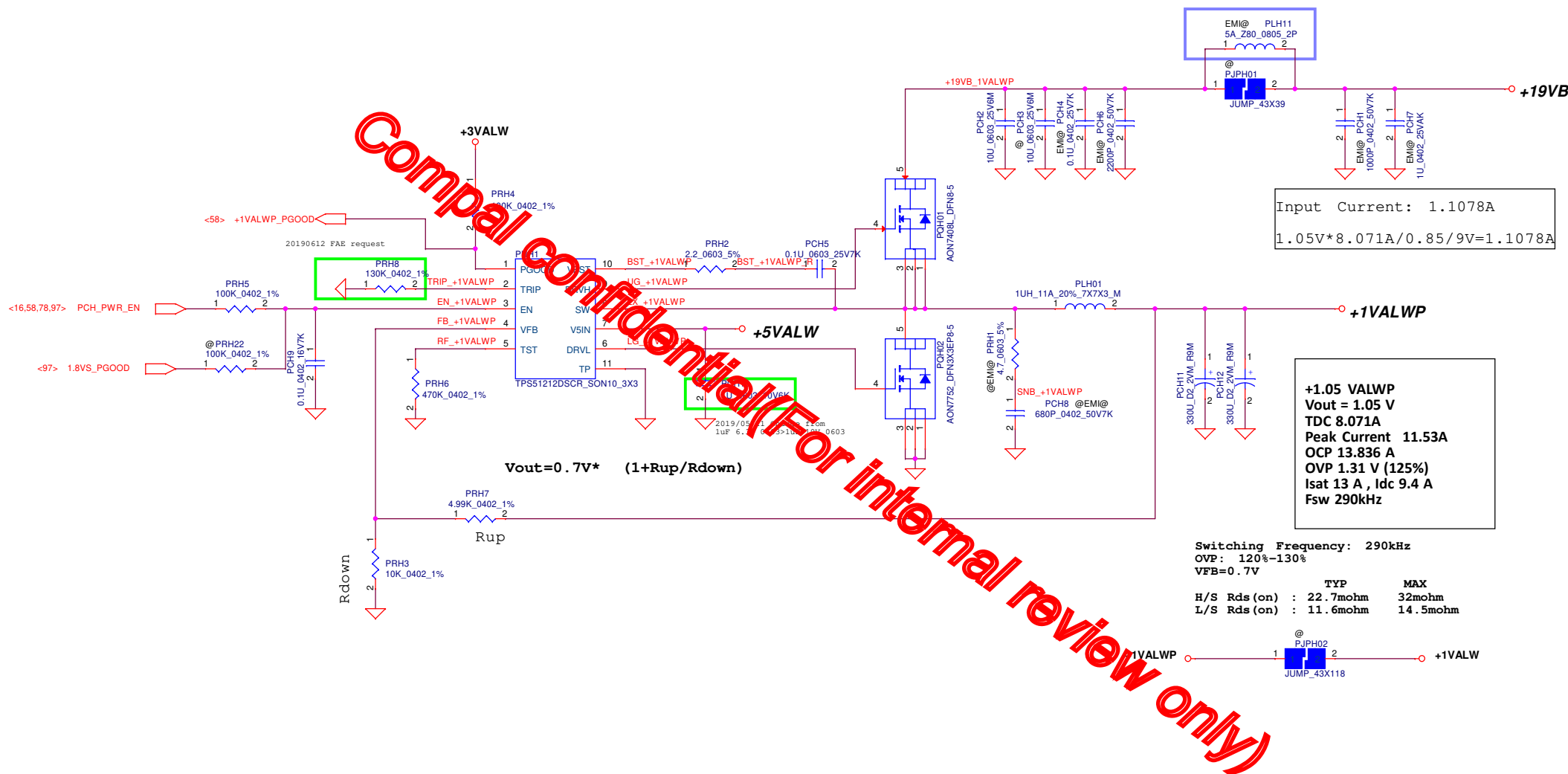
Note: S3 - sleep ; S5 - power off

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title	
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				Size Document Number	
				LA-J521P	
				Date: Wednesday, April 08, 2020	Sheet 87 of 114

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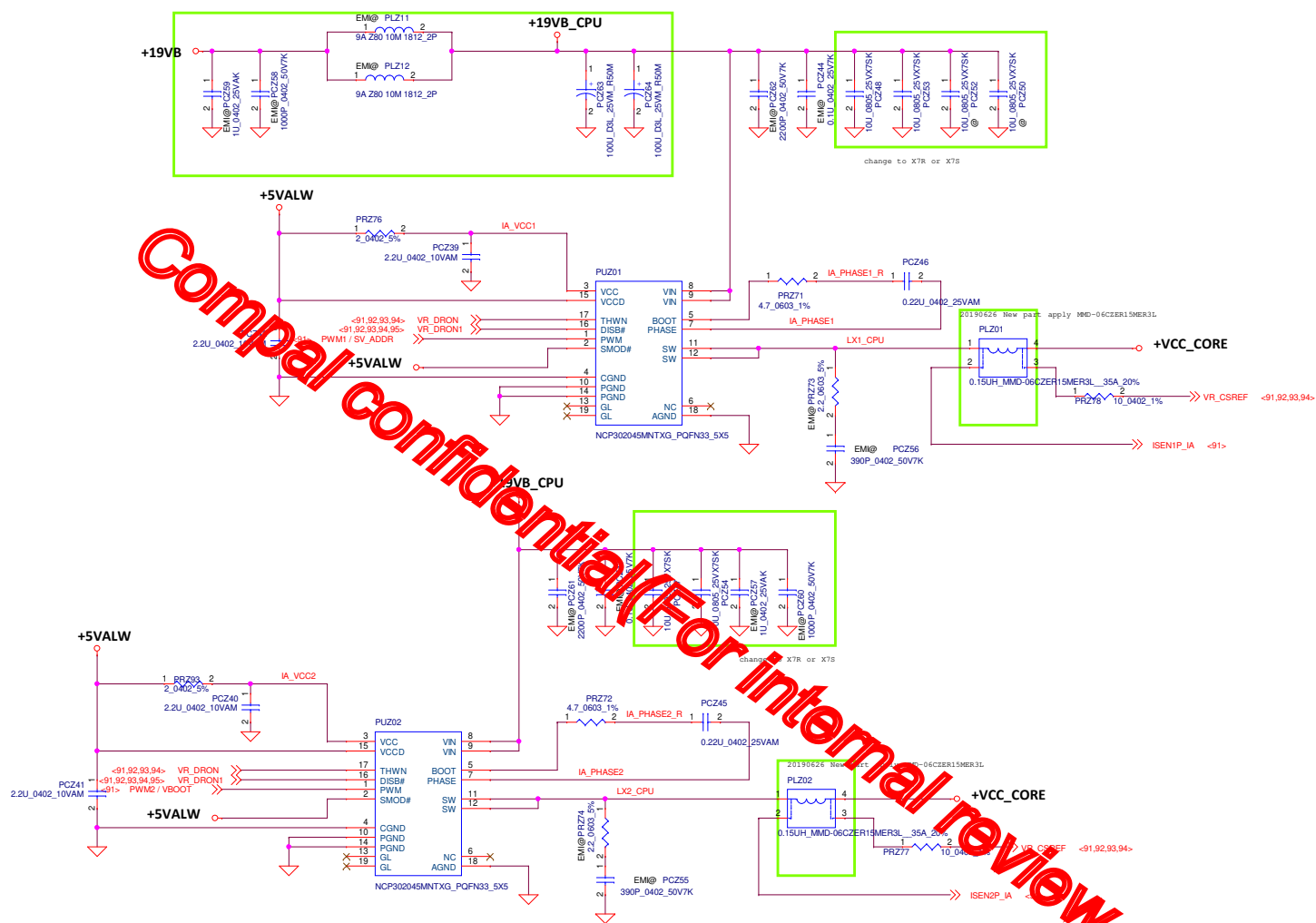
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title					
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				Size			Document Number		Rev
				LA-J521P			Date		0.3
				Wednesday, April 08, 2020			Sheet		88 of 114



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Issued Date		2018/05/16		Deciphered Date		2018/12/31		Title			
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						Size		Document Number		Rev	
								LA-J521P		0.3	
						Date:		Wednesday, April 08, 2020		Sheet 89 of 114	

Main Func = CORE_Phase1&2

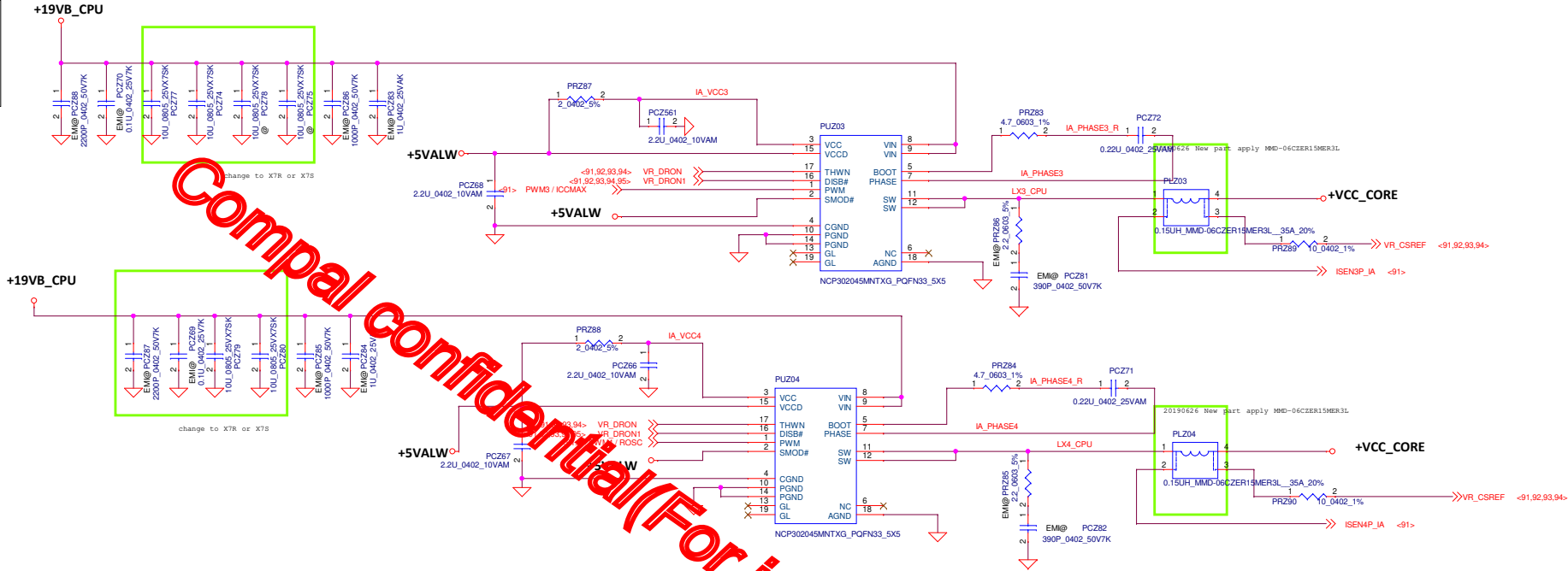
+VCC_CORE
TDC PL2 :146A
Peak Current 192A
OCP Current 230A
DCR mohm +/-5%



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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				Size	Document Number
				LA-J521P	
Date: Wednesday, April 06, 2020		Sheet		92	of 114

Main Func = CORE_Phase3&4

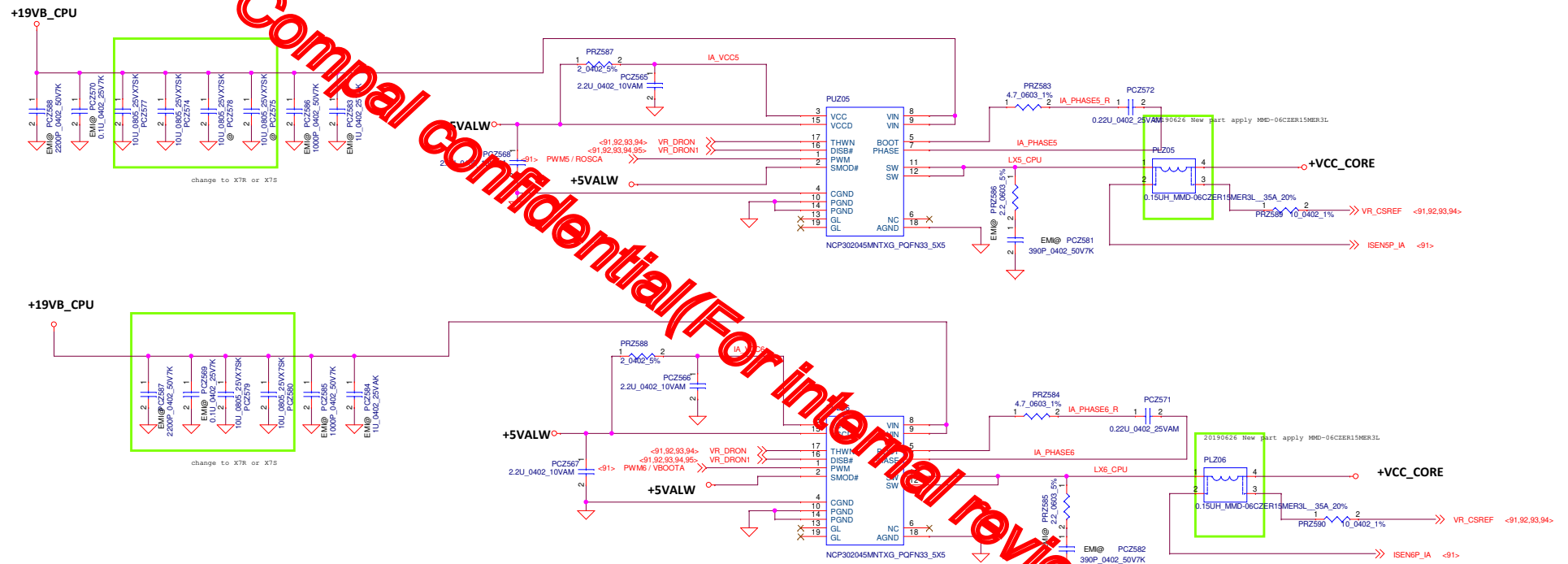
+VCC_CORE
TDC PL2 :146A
Peak Current 192A
OCP Current 230A
DCR mohm +/-5%



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	+VCC_CORE Phase3&4		
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				Date	Wednesday, April 08, 2020	Sheet 93 of 114

Main Func = CORE_Phase3&4

+VCC_CORE
TDC PL2 :146A
Peak Current 192A
OCP Current 230A
DCR mohm +/-5%



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title		Rev 03
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					LA-J521P	
				Date:	Wednesday, April 06, 2020	Sheet 94 of 114

+VCC CORE

470U D2 2.5VM R4.5M
PCZ400

VIBER +VCC CORE
470uF D2 x5
22uF 0805 x48 (footprint NPM)
22uF 0603 x48
10uF 0603 x35
1uF 0201 x48

+VCCGT

+VCCGT
470uF D2 x1
22uF 0805 x21 (Footprint NPM)
22uF 0603 x21

+VCCSA

VIBER +VCCSA
22uF 0805 x11
220uF D7 X 11

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X7S Change to X7T Part number applying

X7S Change to X7T Part number applying

X7S Change to X7T Part number applying

+VCC CORE

X7S Change to X7T Part number applying

Security Classification
Issued Date
2018/05/16
Deciphered Date
2018/12/21
Title
PWR CPU DECOUPLING
Doc Number
LA-1521P
Date
Wednesday, 12/21/2018
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of
114

Compul Electronics, Inc.

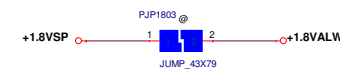
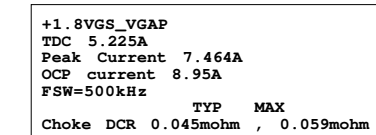
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Component List:

- IC: SY8386RHC-QFN16 2P5X2P5
- Capacitors: PC1812 (4.7uF 0.402 10V 5%), PC1810 (22uF 0.603 5.3V 5%), PC1811 (22uF 0.603 5.3V 5%), PC1813 (10k 0.402 5%), PC1814 (10k 0.402 5%), PC1815 (10k 0.402 5%), PC1816 (2.2uF 0.402 5.3V 5%), PC1817 (0.1uF 0.603 25V 7K), PC1818 (0.1uF 0.402 16V 7K), PC1819 (10k 0.402 5%), PC1820 (880pF 0.402 50V 7K), PC1821 (0.1uF 0.402 16V 7K), PC1822 (0.1uF 0.402 16V 7K).
- Resistors: PR1808 (0.0603 5%), PR1809 (18.2K 0.001 1%), PR1810 (22uF 0.603 5.3V 5%), PR1811 (22uF 0.603 5.3V 5%), PR1812 (4.7uF 0.402 10V 5%), PR1813 (10k 0.402 5%), PR1814 (10k 0.402 5%), PR1815 (10k 0.402 5%), PR1816 (2.2uF 0.402 5.3V 5%), PR1817 (0.1uF 0.603 25V 7K), PR1818 (0.1uF 0.402 16V 7K), PR1819 (10k 0.402 5%), PR1820 (880pF 0.402 50V 7K), PR1821 (0.1uF 0.402 16V 7K), PR1822 (0.1uF 0.402 16V 7K).
- Inductor: PL1802 (1uH MMD-054H-N1 FROM-X2L 8A 20%).
- Diode: D1801 (180V 0.402 5%).
- Signal: 1.8VSP_PGOOD (-89%).

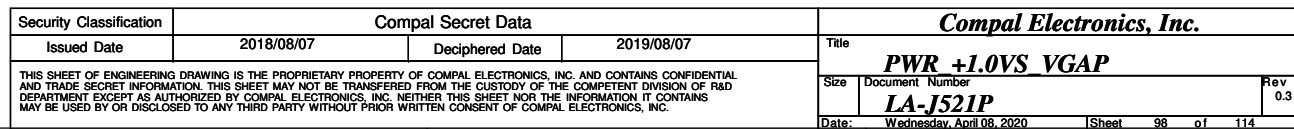
Output Regulation:

- Vout = 0.6V* (1 + Rup/Rdown)
- Load Regulation: 16.58, 78.89%



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Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title	
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					LA-521P
				Date:	Wednesday, April 08, 2020
				Sheet	97 of 114

```
+1.0VS_VGAP
Vout=1.0V
TDC=4.7A
Peak Current      6.7A
OCP current      8A
FSW=1MHz
                TYP      MAX
Choke DCR      0.045mohm , 0.070mohm
```



+VDDCR_GFX
TDC 180A
Peak Current 450A
OCP current A
FSW=450kHz

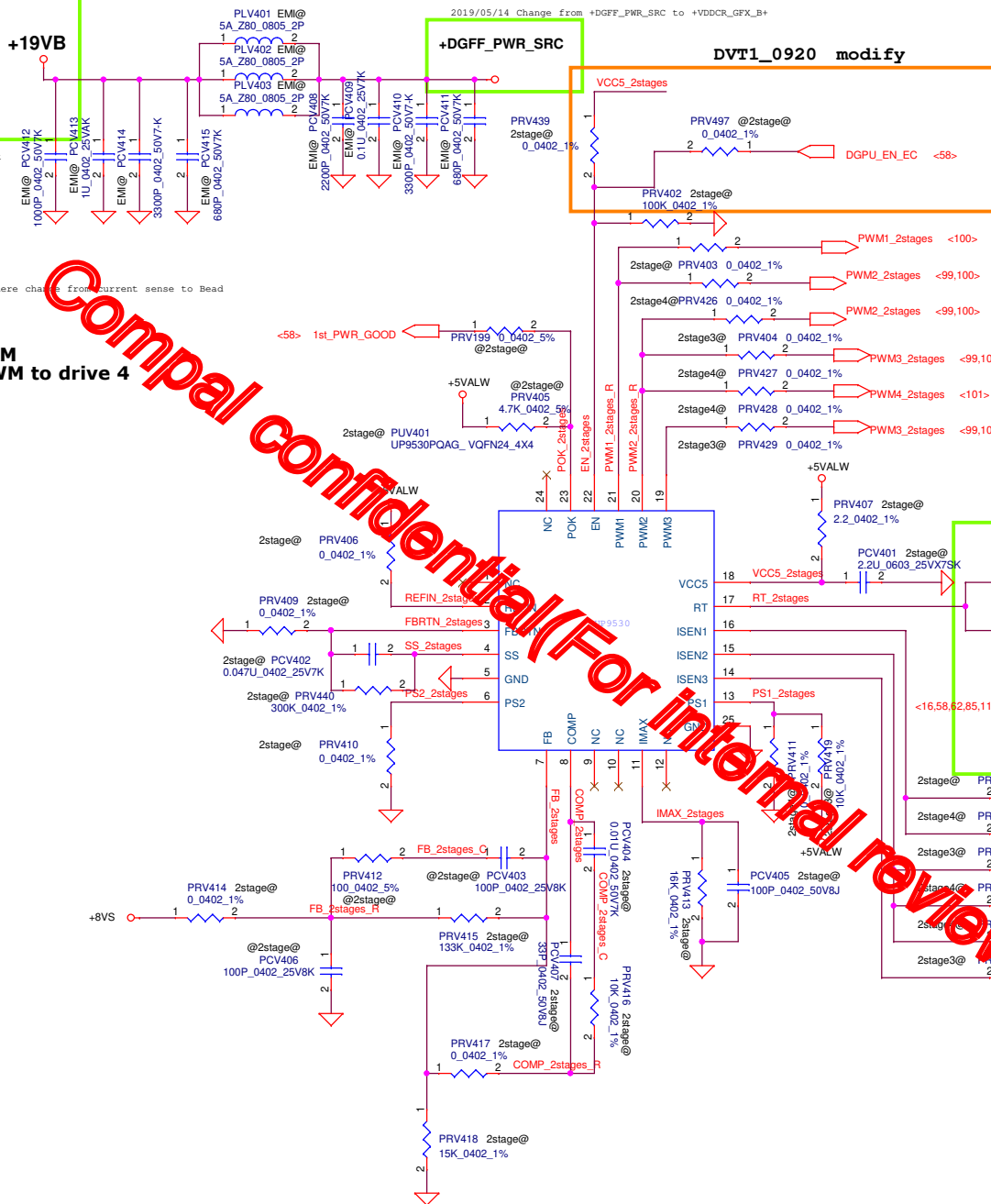
2019/05/14 because typec and barrel input
here change from PJPDC1 connector to B+

2019/05/14 because AMD no support CSSN and CSSP here change from current sense to Bead

UP9530 3phase and 4phase BOM
3phase 4phase (2PWM to drive 4

Dr.MOS	10kohm	x	0ohm
PRV419	x	0ohm	0ohm
PRV411	0ohm	x	0ohm
PRV403	x	0ohm	0ohm
PRV426	0ohm	x	0ohm
PRV404	x	0ohm	0ohm
PRV427	x	0ohm	0ohm
PRV428	x	0ohm	0ohm
PRV429	0ohm	x	0ohm
PRV420	0ohm	x	0ohm
PRV421	0ohm	x	0ohm
PRV422	0ohm	x	0ohm
PRV423	x	0ohm	0ohm
PRV424	x	0ohm	0ohm
PRV425	0ohm	x	0ohm
PRV119	2kohm	3.9kohm	
PRV125	2kohm	3.9kohm	
PRV131	2kohm	3.9kohm	
PRV137	x	3.9kohm	

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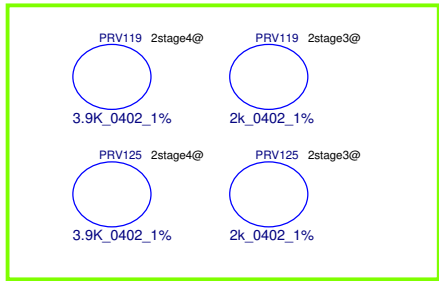
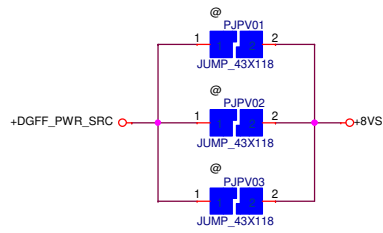
Input Current (Total) : 36.6 A
 $35A * 8V / 0.85 / 9V = 36.6A$

+8VS
TDC 35 A
Peak Current 50 A
OCP 80 A
Isat 50 A , Idc 35 A
Fsw 300k Hz

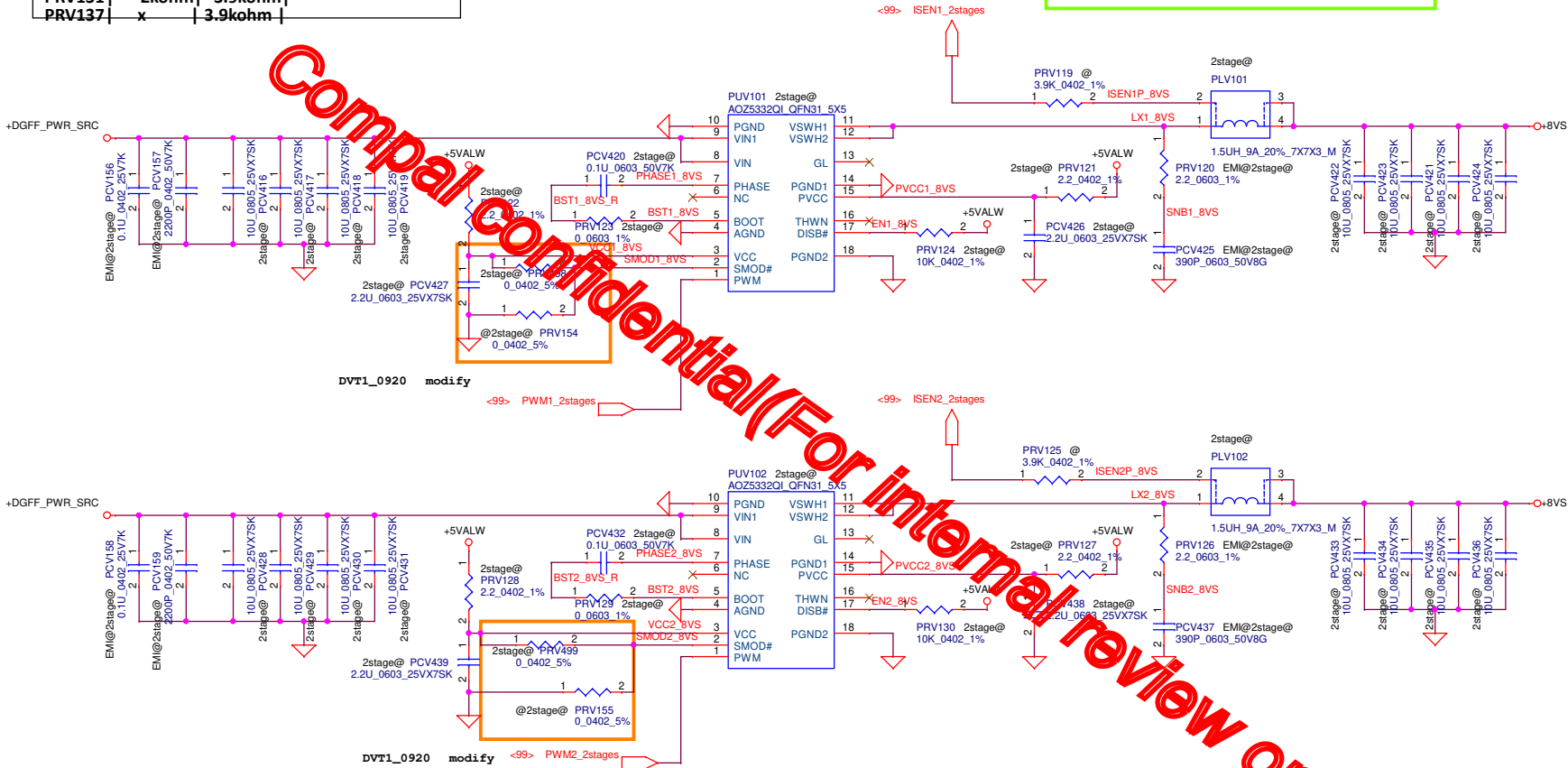
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2019/04/19		Deciphered Date		2020/04/19		Title	
										PWR UP9530 Controller	
										LA-J521P	
										Rev 0.3	
										Date: Wednesday, April 08, 2020	
										Sheet 99 of 114	

Input Current (Total) : 36.6 A
35A * 8V / 0.85 / 9V=36.6A

UP9530 3phase and 4phase BOM			
		3phase	4phase (2PWM to drive 4
Dr.MOS			
PRV119	2kohm	3.9kohm	
PRV125	2kohm	3.9kohm	
PRV131	2kohm	3.9kohm	
PRV137	x	3.9kohm	

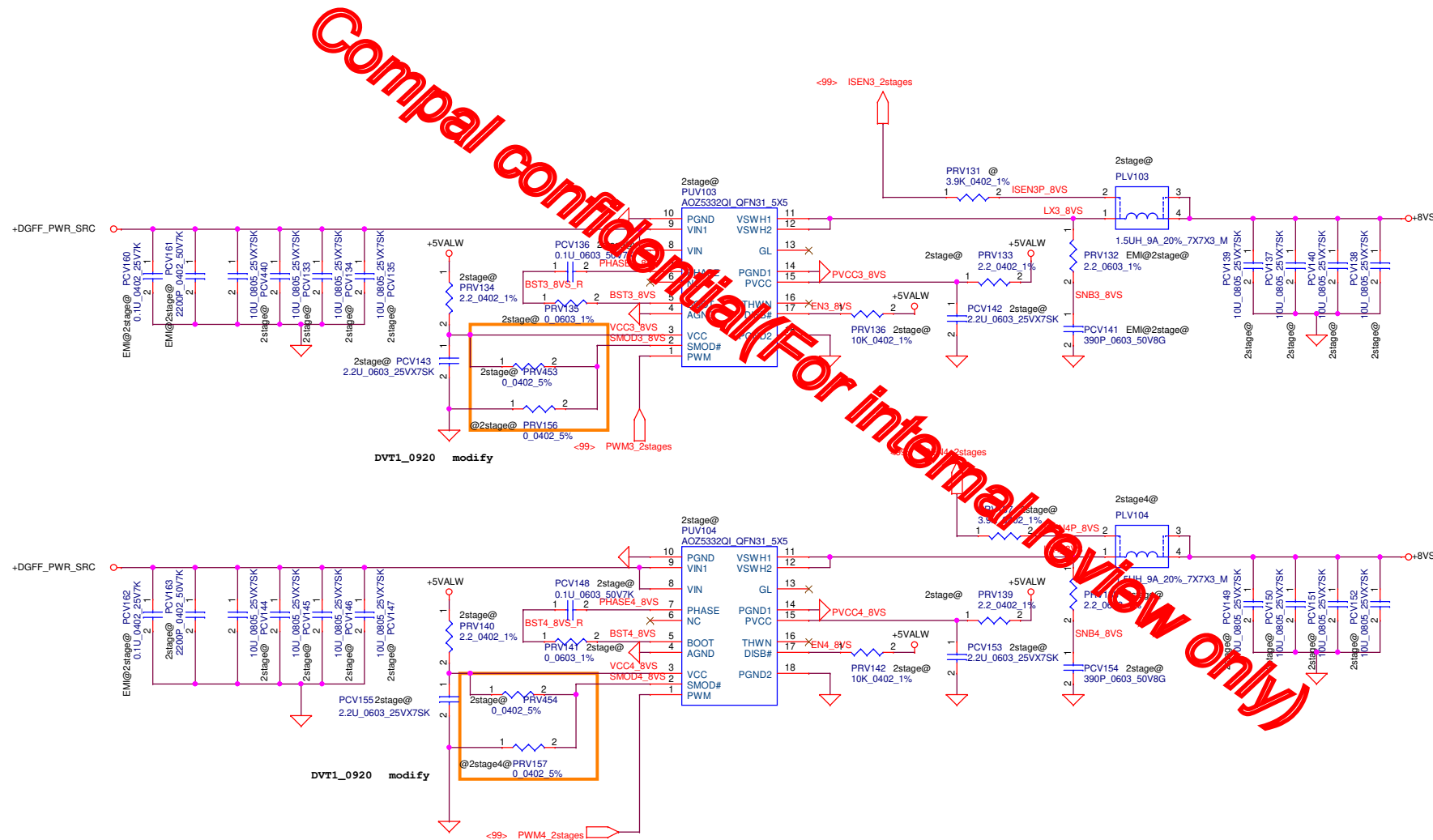
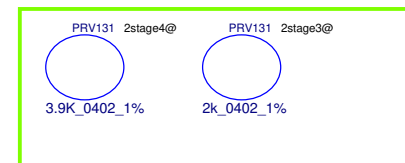


+8VS
TDC 35 A
Peak Current 50 A
OCP 80 A
Isat 50 A , Idc 35 A
Fsw 300k Hz



$$35A * 8V / 0.85 / 9V = 36.6A$$

+8VS
TDC 35 A
Peak Current 50 A
OCP 80 A
Isat 50 A , Idc 35 A
Fsw 300k Hz



Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR 2 stages LA-J521P	
Issued Date	2019/04/19	Deciphered Date	2020/04/19	Title	
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				Date: Wednesday, April 08, 2020	Sheet 101 of 114

OCV setting

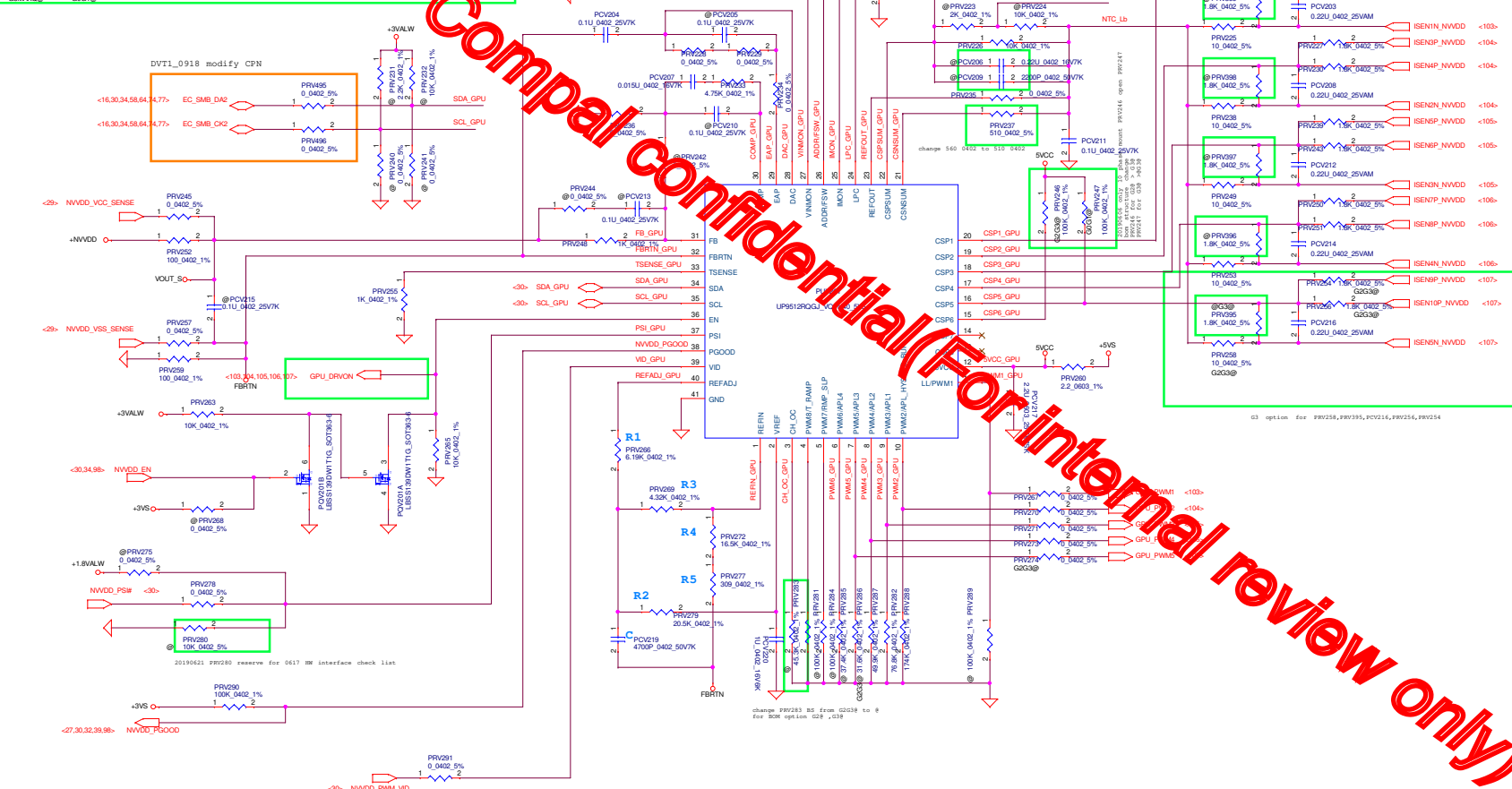


+NVVDD (N18E - G3RMAXP)
TDC 180 A
Peak Current 390A
OCV 480A
OVP 1.43 V
Isat 50 A, I_{dc} 25.1 A
Fsw 300k Hz

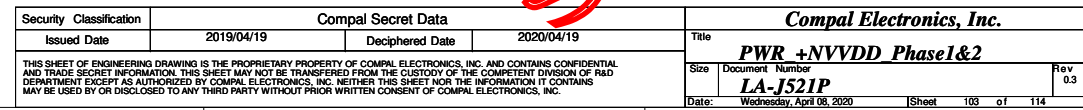
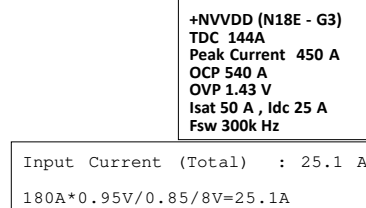
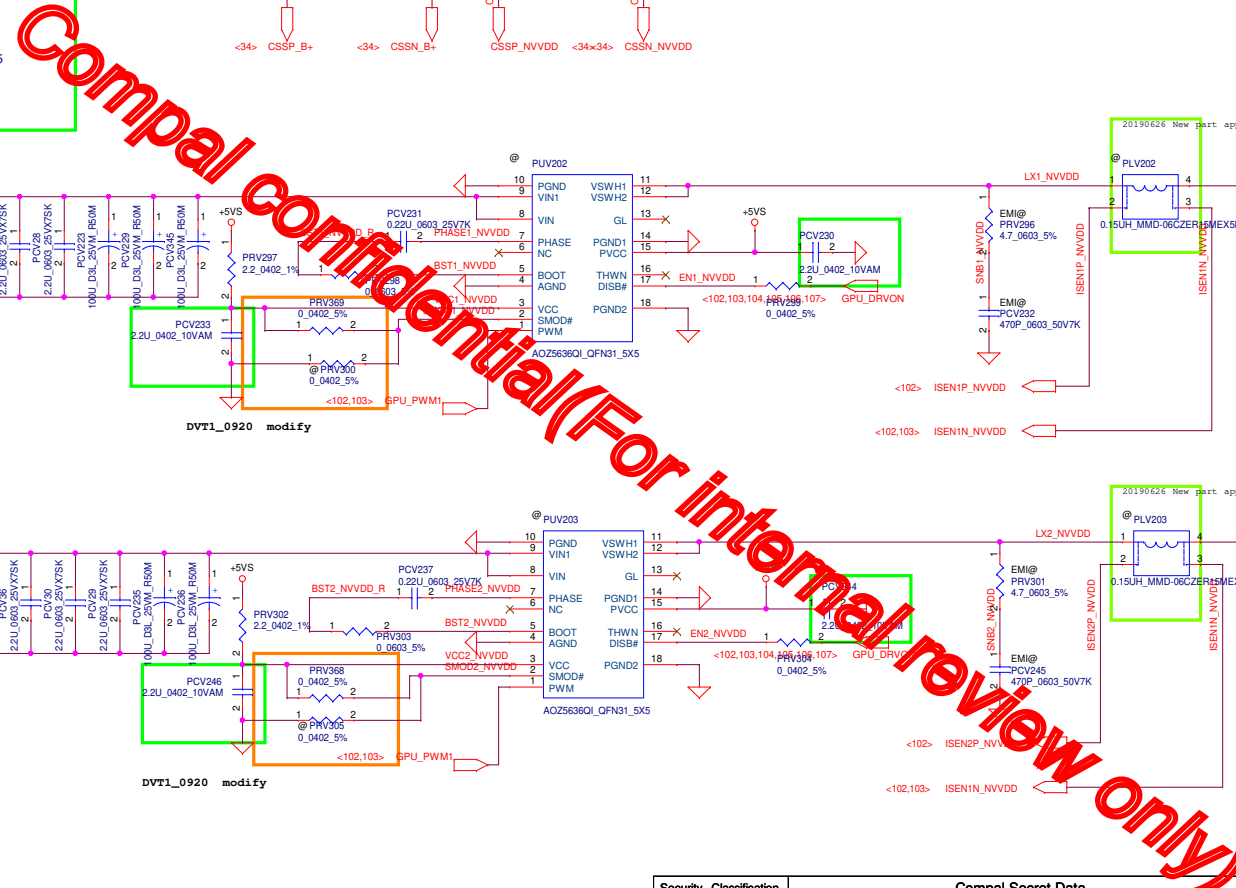
UP9512 8phase and 10phase BOM

8phase	10phase
PRV202 44.2kOhm (270A OCP for G0G1)	36kOhm (145A OCP for G3RMAXP) 43kOhm (145A OCP for G3RMAXP) 54kOhm (160A OCP for G3RMAXP) 56kOhm (160A OCP for G3RMAXP) 58kOhm (160A OCP for G3RMAXP)
PRV214 X	15kOhm
PRV215 X	15kOhm
PRV246 X	10kOhm
PRV247 100kOhm	X
PRV258 X	10kOhm
PRV254 X	1.8kOhm
PRV256 X	1.8kOhm
PCV216 X	0.1uF (Follow firstly change to 0.22uF)
PRV283 51.7kOhm (56.5A per phase OCP for G0G1) (56.5A per phase OCP for G3RMAXP) (56.5A per phase OCP for G3RMAXP) (56.5A per phase OCP for G3RMAXP) (56.5A per phase OCP for G3RMAXP)	56kOhm (125A per phase OCP for G3RMAXP) 58kOhm (125A per phase OCP for G3RMAXP) 60kOhm (125A per phase OCP for G3RMAXP) 62kOhm (125A per phase OCP for G3RMAXP) 64kOhm (125A per phase OCP for G3RMAXP) 66kOhm (125A per phase OCP for G3RMAXP) 68kOhm (125A per phase OCP for G3RMAXP) 70kOhm (125A per phase OCP for G3RMAXP) 72kOhm (125A per phase OCP for G3RMAXP) 74kOhm (125A per phase OCP for G3RMAXP) 76kOhm (125A per phase OCP for G3RMAXP) 78kOhm (125A per phase OCP for G3RMAXP) 80kOhm (125A per phase OCP for G3RMAXP) 82kOhm (125A per phase OCP for G3RMAXP) 84kOhm (125A per phase OCP for G3RMAXP) 86kOhm (125A per phase OCP for G3RMAXP) 88kOhm (125A per phase OCP for G3RMAXP) 90kOhm (125A per phase OCP for G3RMAXP) 92kOhm (125A per phase OCP for G3RMAXP) 94kOhm (125A per phase OCP for G3RMAXP) 96kOhm (125A per phase OCP for G3RMAXP) 98kOhm (125A per phase OCP for G3RMAXP) 100kOhm (125A per phase OCP for G3RMAXP)
PRV223 2.5kOhm	25kOhm
PRV224 10kOhm	10kOhm
PCV206 0.1uF	0.22uF
PCV209 0.1uF	0.022uF

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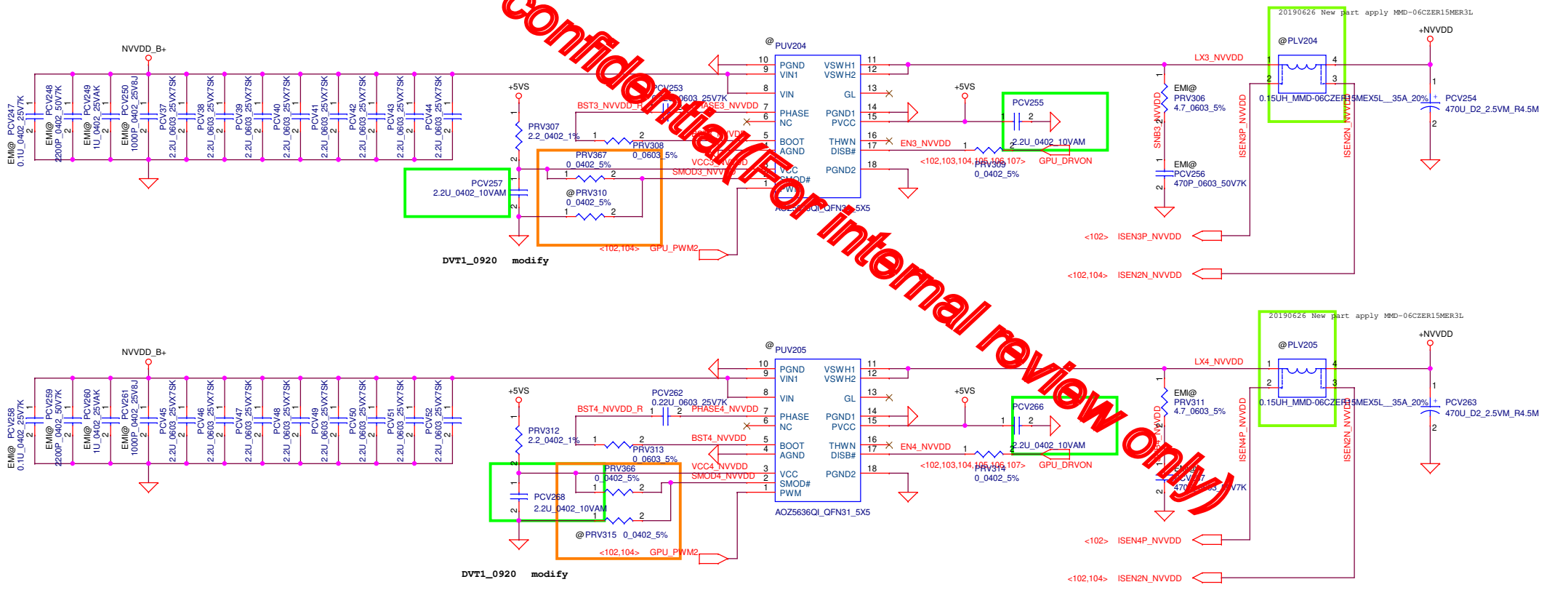
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+NVVDD (N18E - G3)
TDC 180 A
Peak Current 450 A
OCP 540 A
OVP 1.43 V
Isat 50 A , Idc 25 A
Fsw 300k Hz

Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$

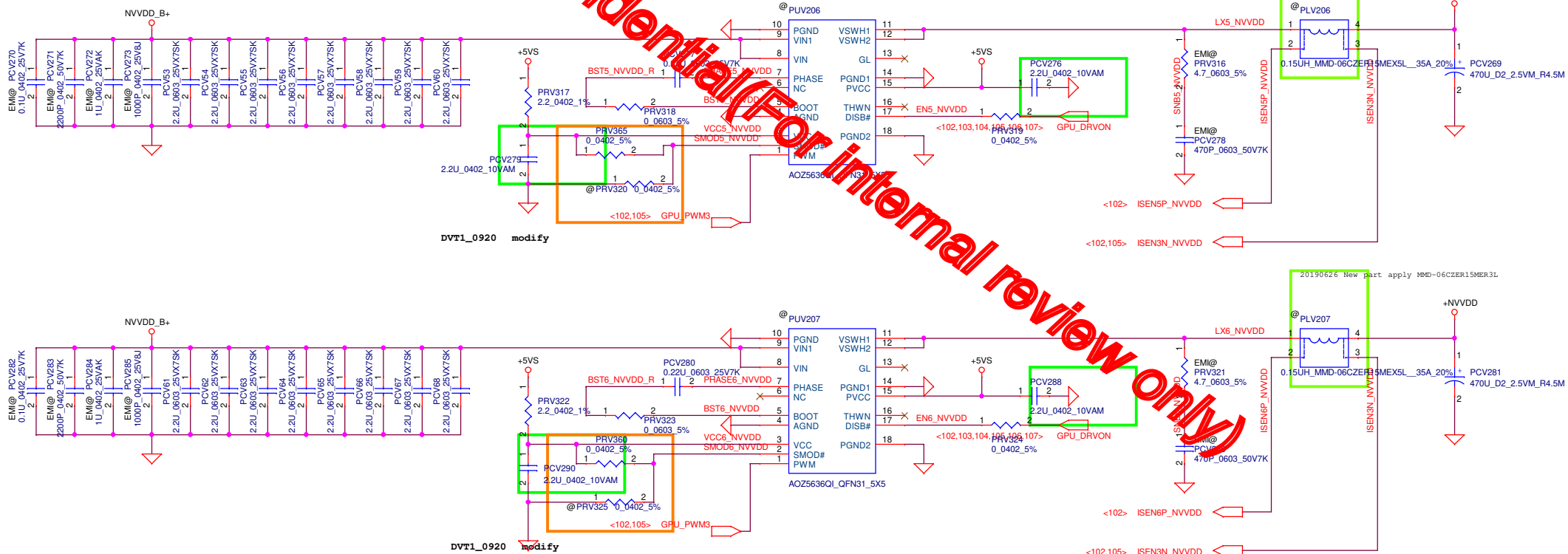


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Size	Document	Number	Rev	LA-J521P	
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+NVVDD (N18E - G3)
TDC 180 A
Peak Current 450 A
OCP 540 A
OVP 1.43 V
Isat 50 A, Idc 25 A
Fsw 300k Hz

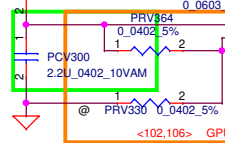
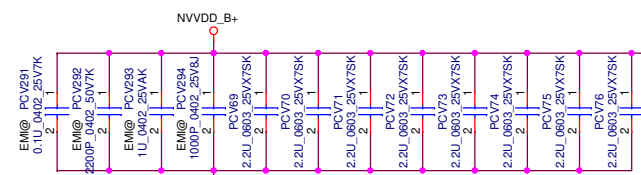
Input Current (Total) : 25.1 A
 $180A \cdot 0.95V / 0.85 / 8V = 25.1A$



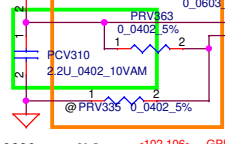
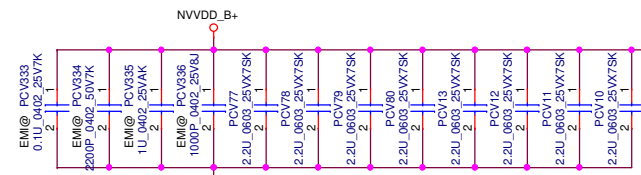
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+NVVDD (N18E - G3)
TDC 180 A
Peak Current 450 A
OCP 540 A
OVP 1.43 V
Isat 50 A, Idc 25 A
Fsw 300k Hz

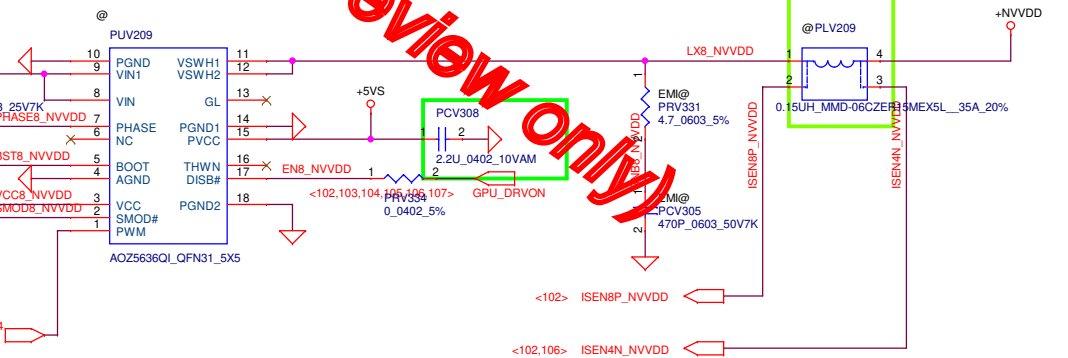
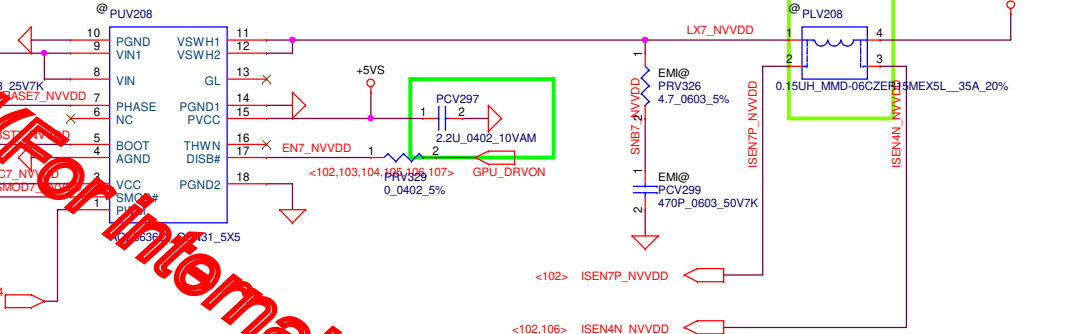
Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$



DVT1_0920 modify



DVT1_0920 modify

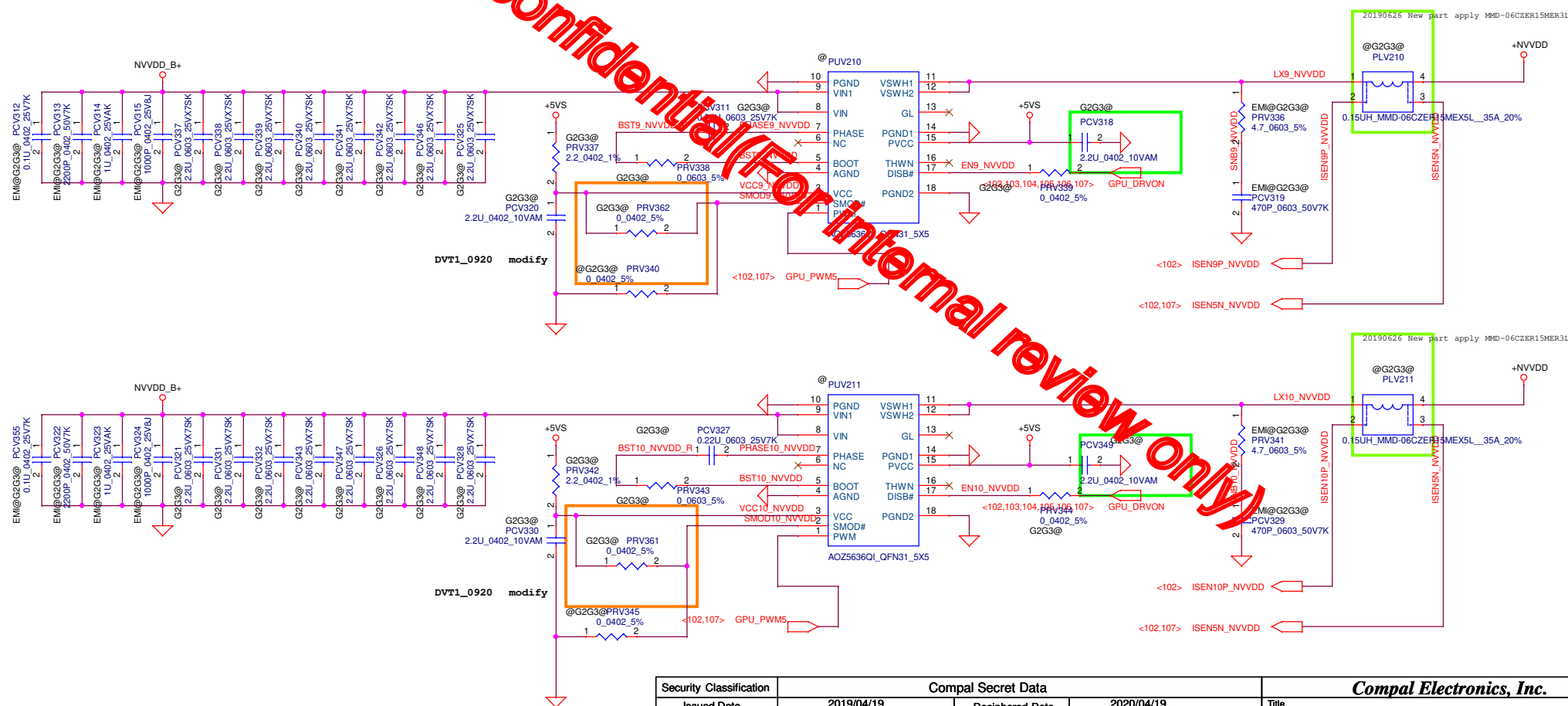


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+NVVDD (N18E - G3)
 TDC 180 A
 Peak Current 450 A
 OCP 540 A
 OVP 1.43 V
 Isat 50 A, Idc 25 A
 Fsw 300k Hz

Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$



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Nvidia Refresh BOM Table									
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
1.35V	V	V	V	V	V	V	V	V	V
1.25V	V	V	V	V	V	V	V	V	V
1.2V	V	V	V	V	V	V	V	V	V

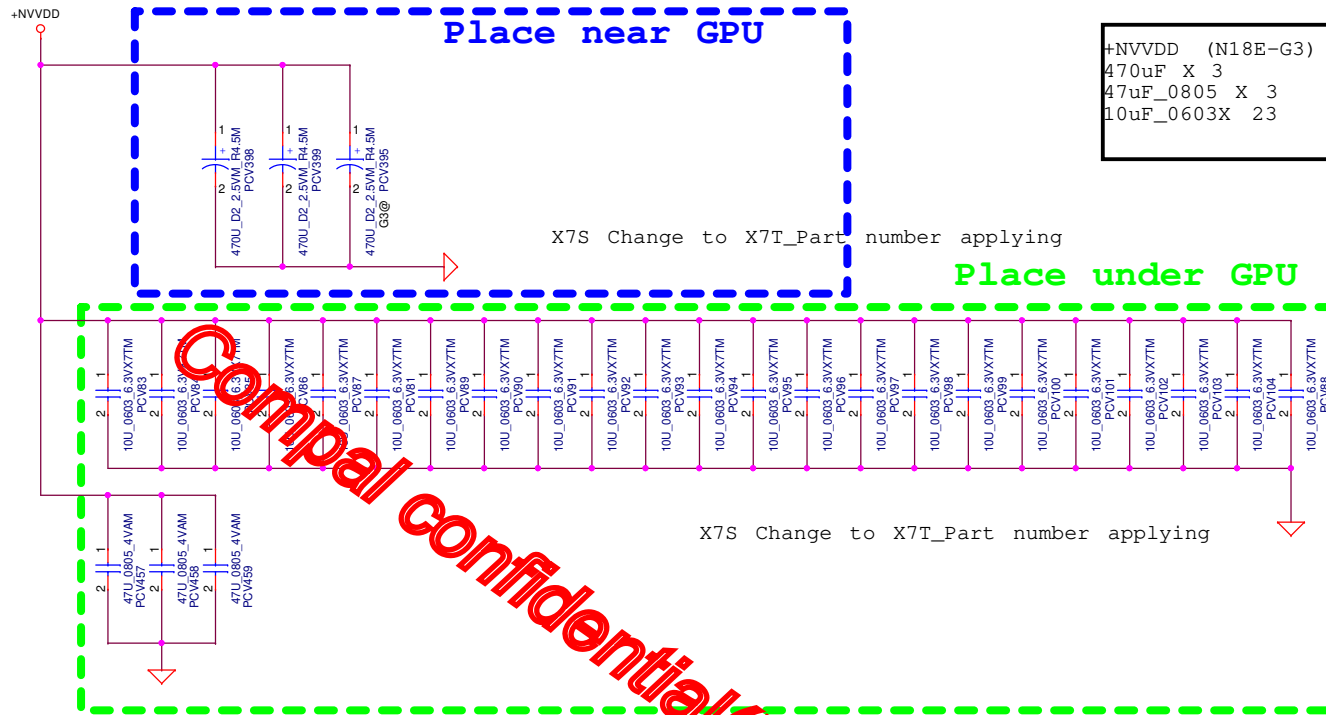
PRW31	NoRefresh@	PRW31	Refresh@	PRW31	G1R@
82.5K_0402_1%		52.3K_0402_1%		140K_0402_1%	
PRW30	G1R@	PRW30	NOG1R@		
16.9K_0402_1%		21K_0402_1%			

PLW2	5332@
AOZ5332QI_QFN31_5X5	
PLW2	5636@
AOZ5636QI_QFN31_5X5	
PLW3	5332@
AOZ5332QI_QFN31_5X5	
PLW3	5636@
AOZ5636QI_QFN31_5X5	

Nvidia Refresh BOM Table 10/05	
1.25V	PRW31
1.2V	PRW31

+1.35VS_VGA
Vout = 1.35V
TDC 46A
Peak Current 66A
OCF current 79.2A
FSW=300KHz
Rdc=0.98 mohm
MAX
H/S Rds (on) : 4.8mohm
L/S Rds (on) : 1.3mohm

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+NVVDD (N18E-G3)
470uF X 3
47uF_0805 X 3
10uF_0603X 23

+NVVDD (N18E-G2)
470uF X3
47uF_0805 X 3
10uF_0603X 23

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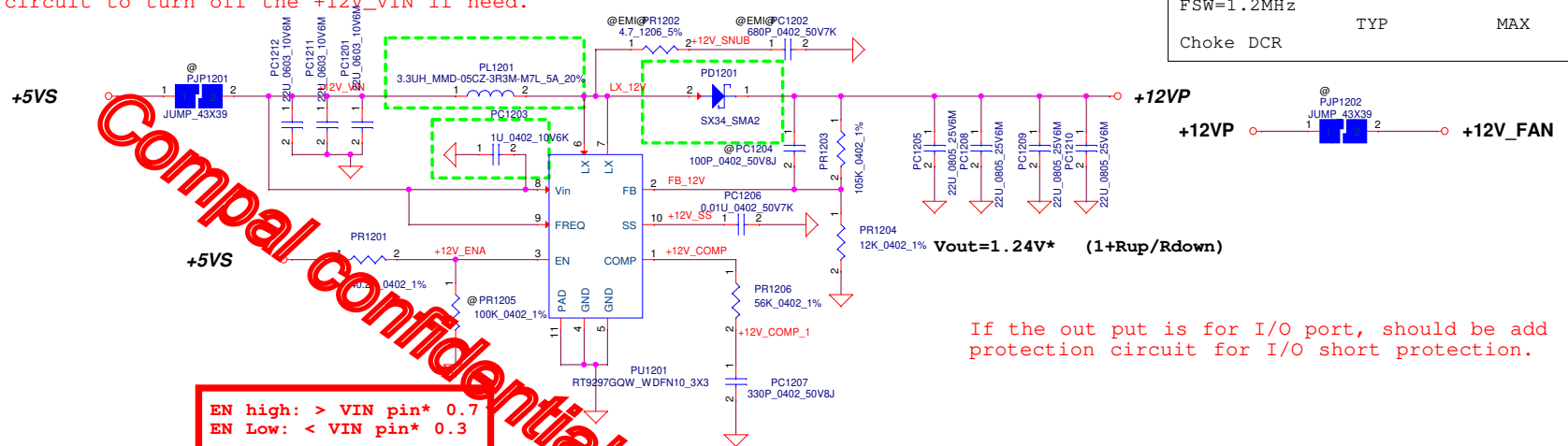
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								Size		Document Number		Rev	
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Input Current: 2.26A
 $12V \times 0.8A / 0.85 / 5V = 2.26A$

+12VP
TDC 0.56A
Peak Current 0.8A
OCP current 3A
FSW=1.2MHz
Choke DCR TYP MAX

Add a switch circuit to turn off the +12V_VIN if need.

Must check PL1201 and PD1201 rating
for your application.



If the out put is for I/O port, should be add
protection circuit for I/O short protection.

FREQ high : Frequency 1.2MHz
FREQ low : Frequency 60KHz

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Vf 1.396V-1.4102V-1.424302V

VIN 4.9952V-5.19V-5.3848V
PD3000 Vf =0.32V@1mA

+3.3V_VDD_DC

PC3002
0.01UF_0402_25V7K

DVT2_1116 modify

AZV3002
Icc=12uA_max
Vout=3.15V@Vcc=3.3V and Io=3mA

PU3001
AZV3002RL7 U-FLGA8_1P65X1P65

PD3001
RB520SM-30T2R_EMD2-2

+VCC_CORE

PR3002 402K_0402_1%
PR3003 30K_0402_1%
@PC3001 82P_0201_50VB
PR3004 200K_0402_1%
PR3005 402K_0402_1%
@PC3003 82P_0201_50VB
PR3007 237K_0402_1%
@PC3008 82P_0201_50VB
BAT54CW_SOT323-3

Vref 0.72V-0.75V-0.78V

PR3010 0402_1%
VCN1_AC_IN <16.58,62.85,99,111>
3.3V+-4% Vf =0.29V@1mA
Ir =1uA @Vr=10V

PC3005 0.22UF_0402_10V6K

DVT1_0918 modify

NO_SMOKE_OVP1

NO_SMOKE_UVP1

DVT1_0918 modify

OV_UV_P1 <58.83,84,111>

VIN 4.9952V-5.19V-5.3848V
PD3000 Vf =0.32V@1mA

Vf 1.9056V-1.98V-2.0544V

+3.3V_VDD_DC

VIN 4.9952V-5.19V-5.3848V
PD3000 Vf =0.32V@1mA

PR3055 43.2K_0402_1%
@PC3055 82P_0201_50VB
BAT54CW_SOT323-3

PR3056 237K_0402_1%
@PC3056 82P_0201_50VB
BAT54CW_SOT323-3

PR3057 147K_0402_1%
PR3058 43.2K_0402_1%
@PC3057 82P_0201_50VB
@PC3058 82P_0201_50VB
BAT54CW_SOT323-3

PR3059 38K_0402_1%
PR3060 30K_0402_1%
@PC3059 82P_0201_50VB
@PC3060 82P_0201_50VB
BAT54CW_SOT323-3

DVT2_1116 modify

AZV3002
Icc=12uA_max
Vout=3.15V@Vcc=3.3V and Io=3mA

PU3051
AZV3002RL7 U-FLGA8_1P65X1P65

PD3054
RB520SM-30T2R_EMD2-2

+NVVDD

DVT2_11231 modify

Vref 0.72V-0.75V-0.78V

DVT1_0918 modify

NO_SMOKE_OVP2

NO_SMOKE_UVP2

DVT1_0918 modify

OV_UV_P1 <58.83,84,111>

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